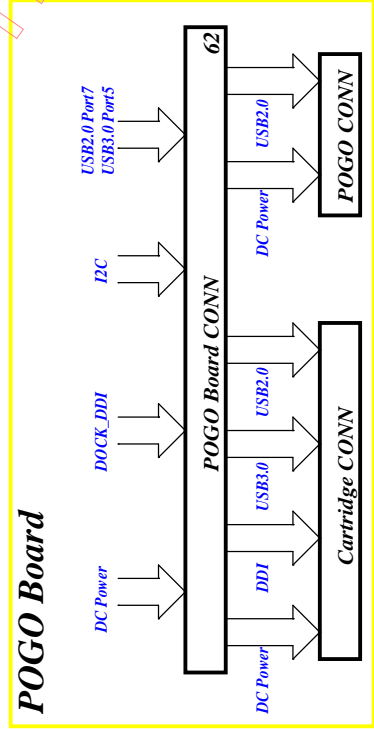
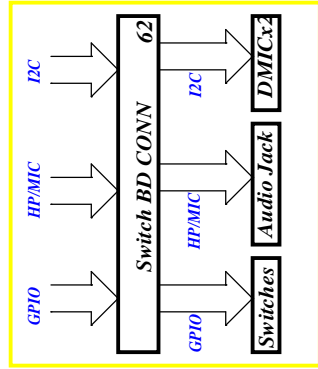
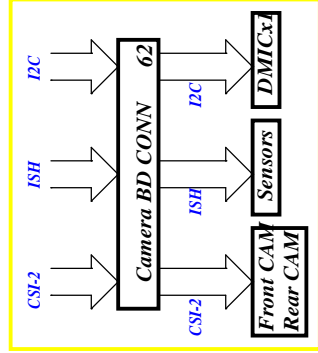
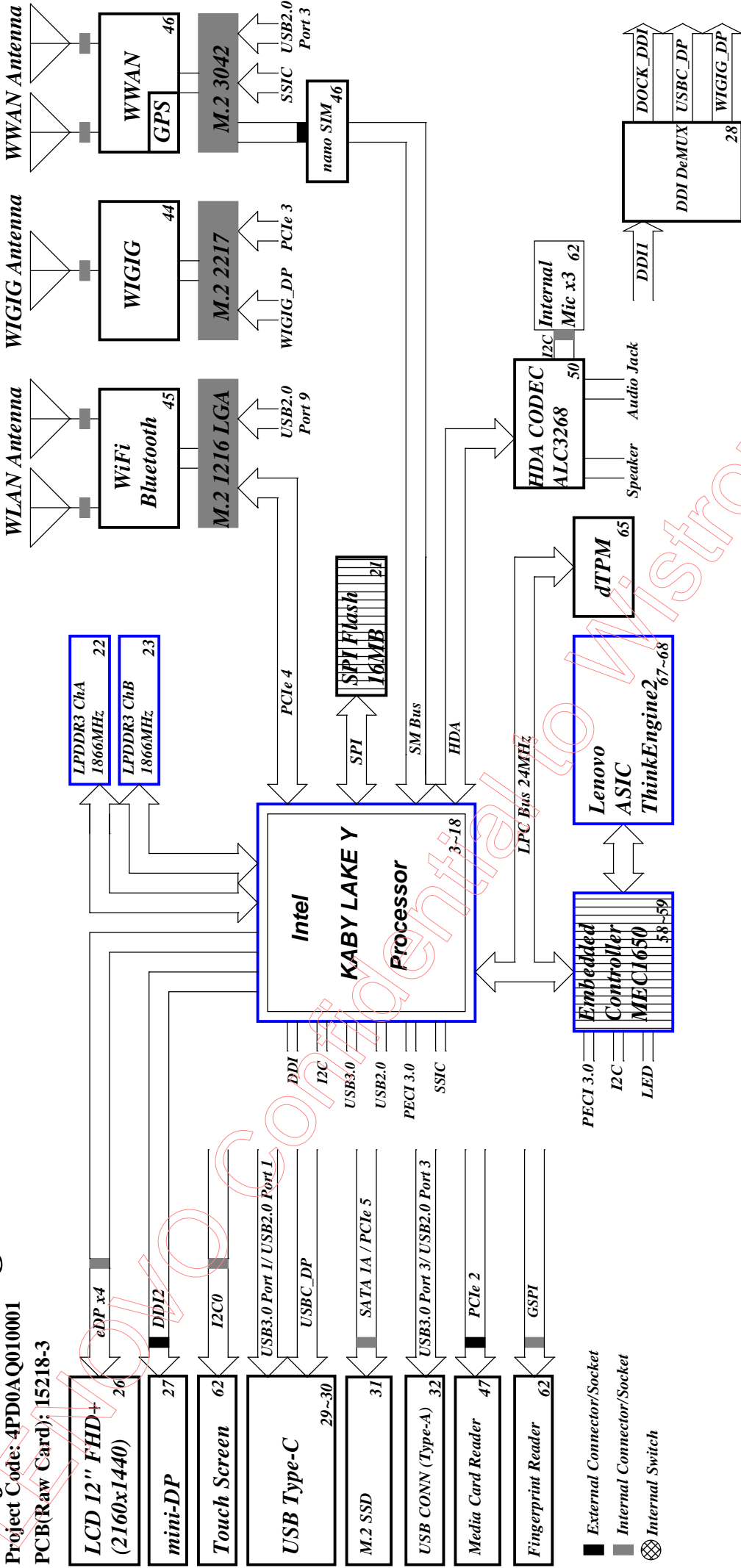


Graf Block Diagram Jul. 07 2016

Project Code: 4PD0AQ010001

PCB(Raw Card): 15218-3



ULX

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Taipei (Taiwan 115), Taiwan, R.O.C.

Block Diagram

Graf-1.5

File

Document Number

Rev

Size

A3

-3

Date

Monday, October 17, 2016

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RESISTOR				
Symbol name	Value	Tolerance	Rating	Size
		(J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	2=>0402, 3=>0603, 5=>0805 6=>1206, 0=>1210

CAPACITOR

Symbol name	Value	Tolerance	Rating	Size
		(M: +/-20, K: +/-10, Z: +80/-20)		2=>0402, 3=>0603, 5=>0805 6=>1206, 0=>1210

PLANAR ID[3.0]

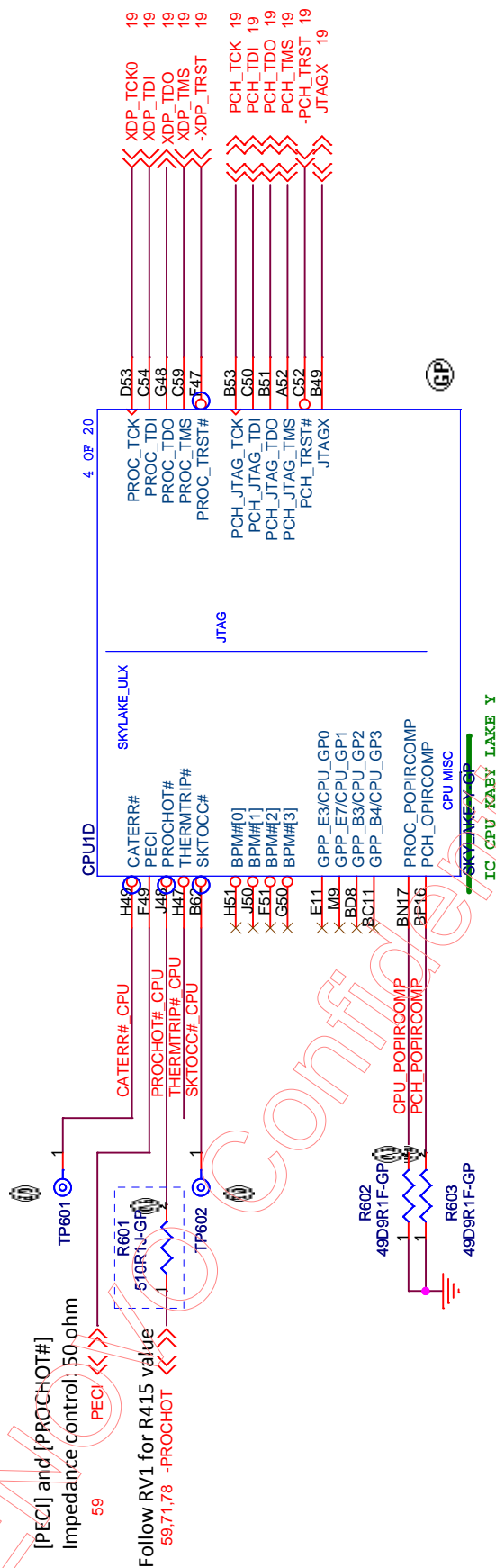
IBEXPEAK-M	PLANAR_IDn	15	14	13	12	Planar ID Version	Planar PCB Version
		3	2	1	0		
		0	0	0	0		
		0	0	0	1	SDV	-2
		0	0	1	0	FVT	-3
		0	0	1	1		
		0	1	0	0		
		0	1	0	1		
		0	1	1	0		
		0	1	1	1		
		1	0	0	0		

[illegible]

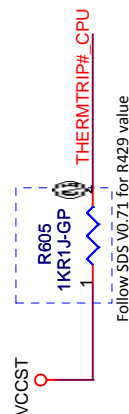
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

EC HISTORY

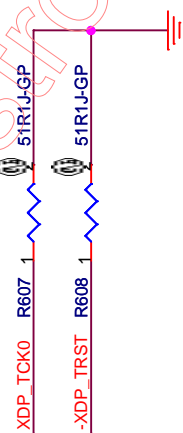
Size A4	Document Number Graf-1.5	Rev -3
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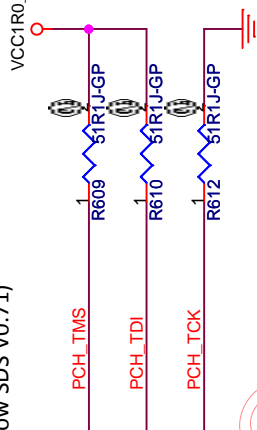
VCCSTG = 1.0 V



PLACE RESISTORS WITHIN 1.1 INCH OF CPU MCP PINS
(follow SDS V0.71)



PLACE RESISTORS WITHIN 1.1 INCH OF PCH MCP PINS
(follow SDS V0.71)



X

通資創緯

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CPU (4/16) : MISC/JTAG

Size	Document Number
------	-----------------

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02

GPP_C5/SMLOALERT# (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

SPI0_MOSI (Boot Halt)	
HIGH	Disable(Default)
LOW	Enable

SPI0_MISO (JTAG ODT Disable)	
HIGH	Enable (Default)
LOW	Disable

SPI0_IO2 (Consent Strap)	
HIGH	Enable (Default)
LOW	Disable

SPI0_IO3 (A0 Personality Strap)	
HIGH	Disable(Default)
LOW	Enable

Table from RV-1, can't find it on EDS and PDG.
Wait for RV team clarify.

RV-1 is PD.

GGPP C2: 1K PU VCC3 SUS for AMT/SBA (-SMB ALERT) same as RV1

法創設

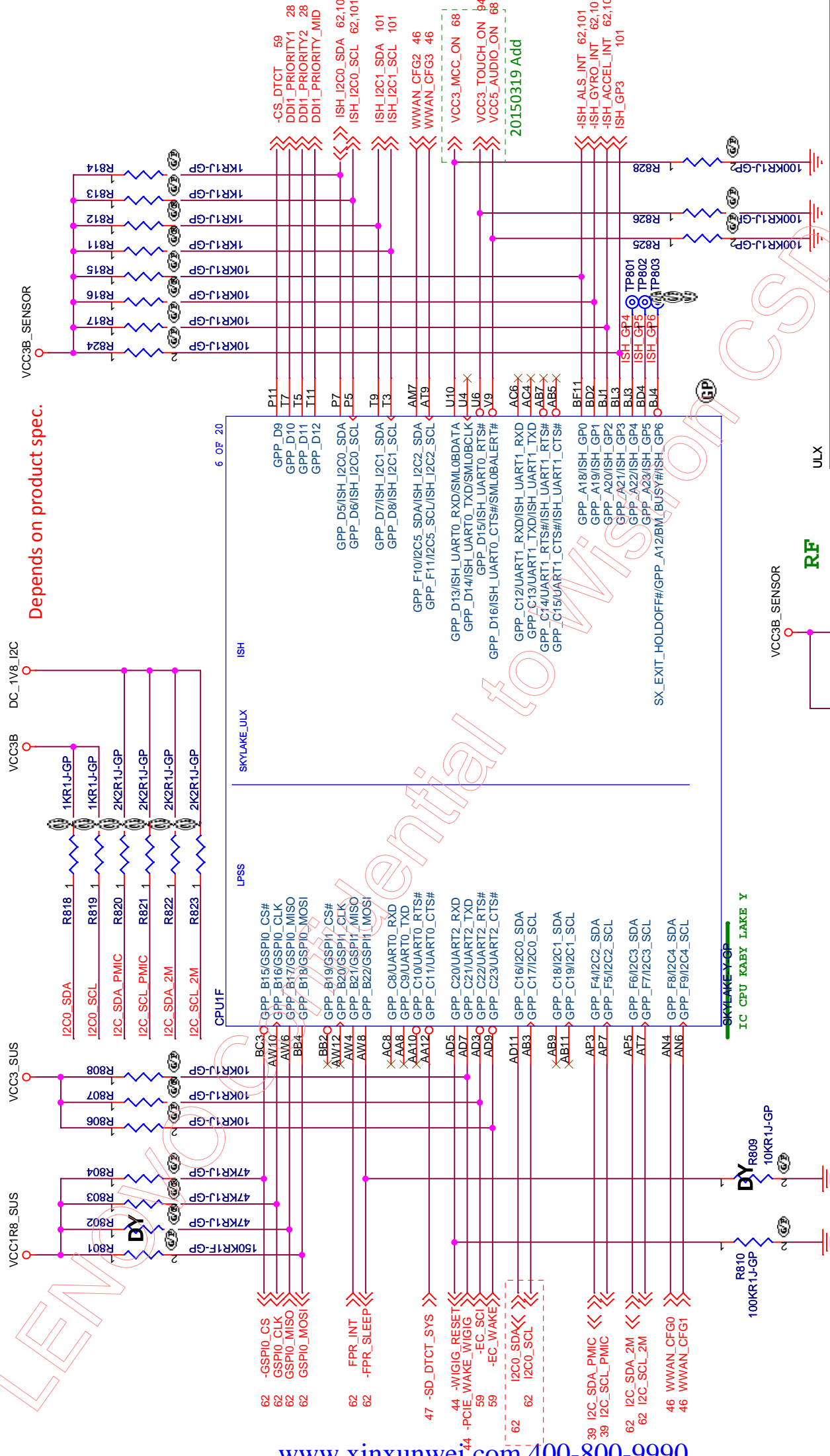
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

CPU(5/16) : LPC/SPI/SMBUS

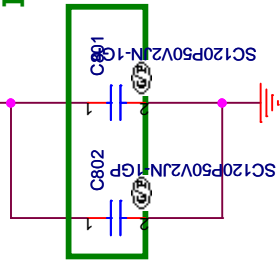
Graf-1.5

Date: Monday, October 17, 2016 Sheet 7 of 102

Depends on product spec.



RF

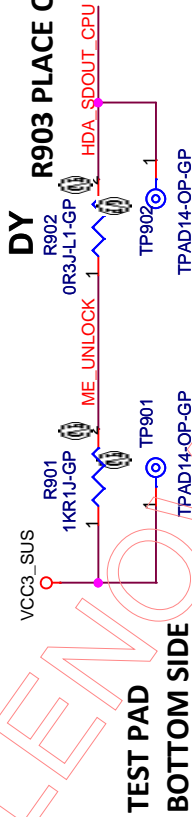


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Title	
CPU (LPSS/ISH/I2C/UART/GPIO)	Rev
Size A4	-3
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Date: Monday, October 17, 2016	
Sheet 8	of 102

DY R903 PLACE ON TOP SIDE



TEST PAD

BOTTOM SIDE

DO NOT MOVE AFTER FIX

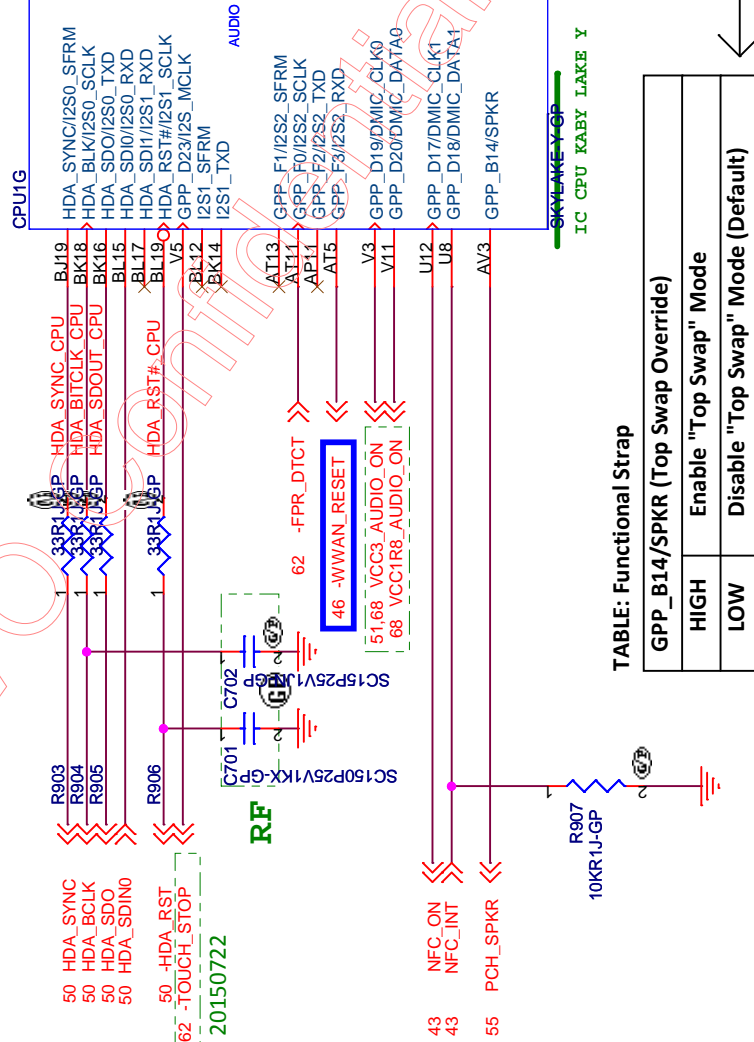


TABLE: Functional Strap

GPP_B14/SPKR (Top Swap Override)		
HIGH	Enable "Top Swap" Mode	
LOW	Disable "Top Swap" Mode (Default)	

LOGIC

38.7 Functional Description

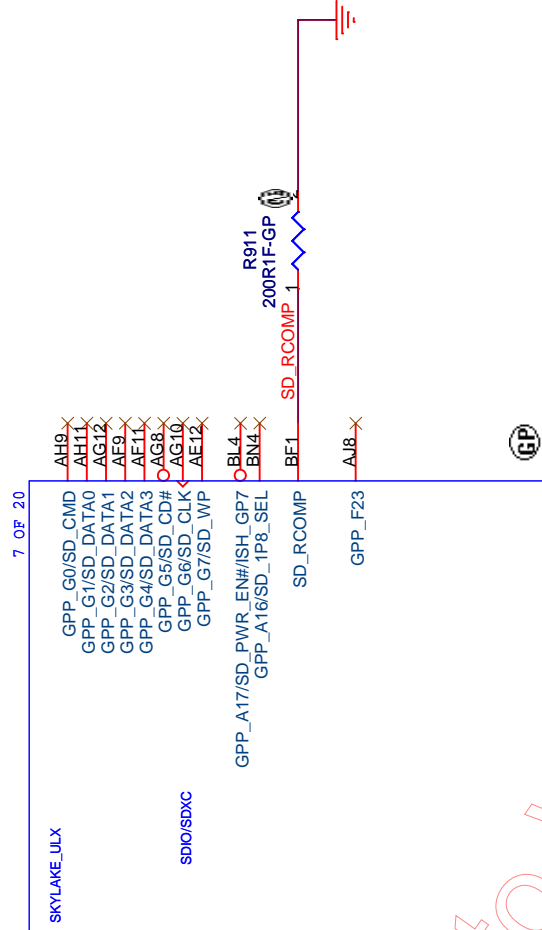
The Controller can function both as a SDIO or SD Card host controller.

SDIO Mode: When configured to SDIO mode, it Handles SDIO Protocol at transmission, packing data, adding cyclic redundancy check (CRC), start/end bit, and checking for transaction format correctness. The SDIO controller main use case it to connect to an external WIFI device.

SD Card Mode: When configured to SD Card Mode it handles SD Protocol at transmission, packing data, adding cyclic redundancy check (CRC), start/end bit, and checking for transaction format correctness. The SD Card main use case is to connect to an external detachable storage device. It support SDIO card specification version 3.0. Both 1.8V and 3.3V signalling is supported. Additional information can be obtained from the SDIO card specification.

TABLE: Functional Strap

HDA_SDO/I2S0_TXD		
Flash Descriptor Security Override		
HIGH	Disable Flash Descriptor Security (Override)	
LOW	Enable Flash Descriptor Security (Default)	



Need Check SD_CD# and SD_WP connection.
*SDIO WIFI don't support Intel AMT.

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Title

CPU(7/16) : AUDIO/SDXC

Size A4

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Flexible I/O Configuration

I/O	High Speed Signals	Configuration	Net Name
Port 1	USB3_1	USB3_1	USB3P1
Port 2	USB3_2/SSIC 1	SSIC 1	SSIC
Port 3	USB3_3/SSIC 2	USB3_3	USB3P3
Port 4	USB3_4	USB3_4	NC
Port 5	USB3_5/PCIE 1	USB3_5	USB3P5
Port 6	USB3_6/PCIE 2	PCIE 2	PCIE2
Port 7	PCIE 3 (GbE)	PCIE_3	PCIE3
Port 8	PCIE 4 (GbE)	PCIE_4	PCIE4
Port 9	PCIE 5 (GbE)	PCIE_5 (x4)	PCIE5_L3
Port 10	PCIE 6	PCIE_6 (x4)	PCIE5_L2
Port 11	PCIE 7/SATA0	PCIE_7 (x4)	PCIE5_L1
Port 12	PCIE 8/SATA1	PCIE_8 (x4) / SATA_1A	PCIE5_L0_SATA1
Port 13	PCIE 9 (GbE)	PCIE_9 (x2)	NC
Port 14	PCIE 10 (GbE)	PCIE_10 (x2)	NC

PCIe Table

Pair	Device
2	Media Card Controller
3	Pine Peak (WiFi)
4	M.2 WLAN
5	M.2 PCIe SSD (x4)
9	NC
10	NC

USB2.0 Table

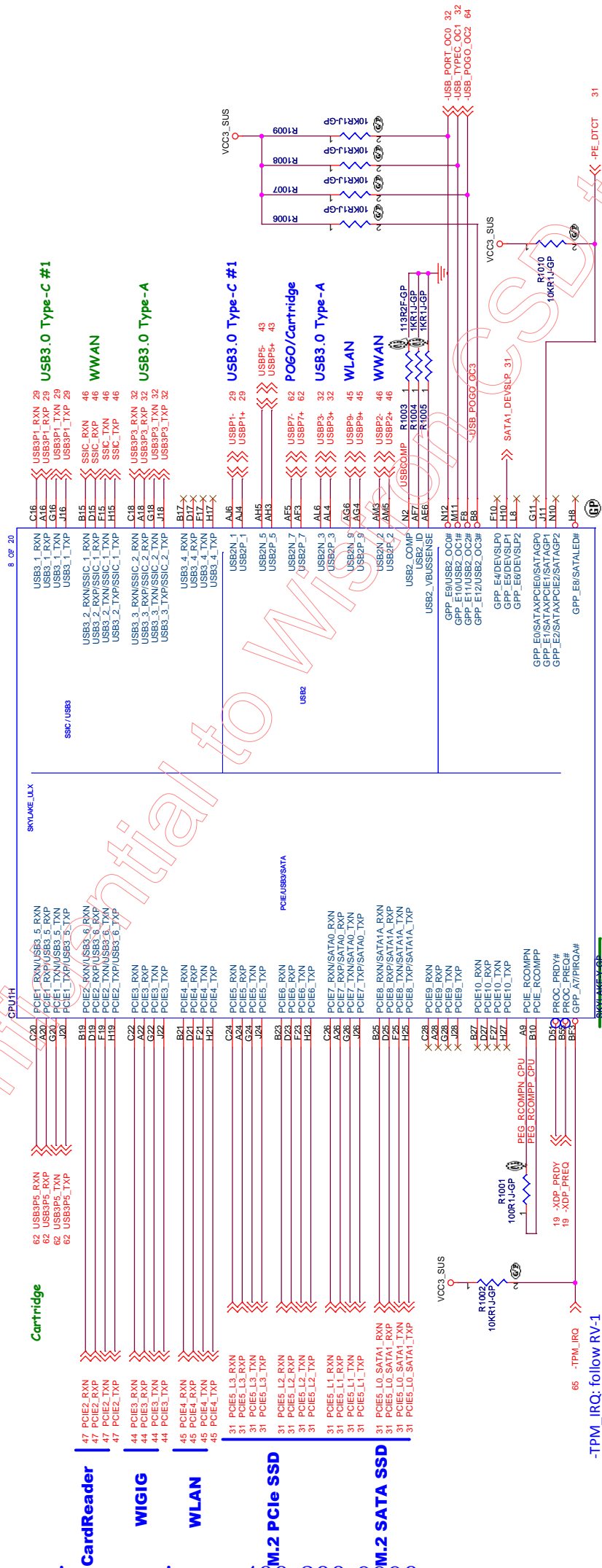
Pair	Device
1	USB3.0 Type-C Port #1
2	M.2 WWAN
3	USB3.0 Type-A Port (Debug)
5	NC
7	Thin-Keyboard, Cartridge
9	M.2 WLAN

SATA Port Assignment

Pair	Device
0	(PCIe9) NC
1A	M.2 SATA SSD

USB3.0 Table

Pair	Device
1	USB3.0 Type-C Port #1
2	M.2 WWAN
3	USB3.0 Type-A Port (Debug)
4	NC
5	Cartridge



-TPM_IRQ: follow RV-1

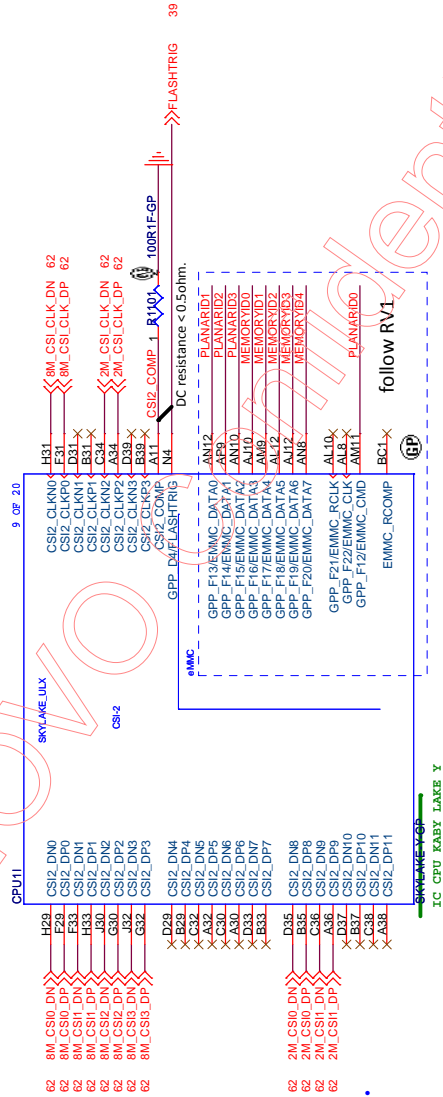
IC CPU EASY LAKE Y

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File
Size
AS
Document Number
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Monday, October 11, 2016
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CPU(8/16) : PCIe/SATA/USB
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-3

MIPI-CSI2 I/F Camera Connection is under confirmation.



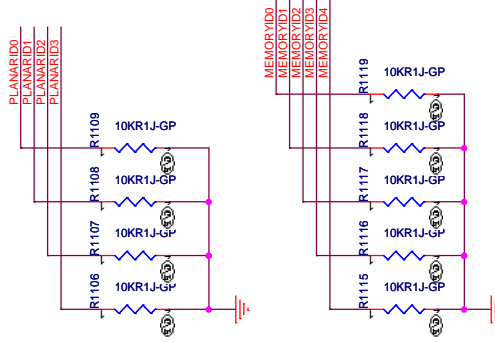
TP should be placed near Soc side with minimum stub.
GND pad should be adjacent to each CSI signal

DEBUG OPTION
FOR MIPI-CSI SI MEASUREMENT

	Supplier	Memory ID0 GPIO F16	Memory ID1 GPIO F17	Memory ID2 GPIO F18	Memory ID3 GPIO F19	Memory ID4 GPIO F20	Supplier P/N	Wistron PN
4GB	Samsung	0	0	0	0	0	K4E8E324EB-EGCF	SM30KS9901AA
	Hynix	0	1	0	0	0	H9CCNNN8GTALAR-NUD	SM30E51293AA
	Micron	1	0	0	0	0	EDF8132A3MA-ID-F	SM30E51262AA
	Micron	1	0	0	0	1	MT52L256M32D1PF-107 WT-B	SM30KS9900AA
8GB	Samsung	0	0	1	0	1	K4E6E304EB-EGCF	SM30KS9893AA
	Hynix	0	1	1	0	0	H9CCNNNB1TALAR-NUD	SM30E51294AA
	Micron	1	0	1	0	0	MT52L512M32D2PF-107 WT-B	SM30KS9888AA
	Samsung	0	0	0	1	0	K4EBE304EB-EGCF	SM30J20264AA
16GB	Hynix	0	1	0	1	1	H9CCNNNCLGALAR-NUD	SM30E51295AA
	Hynix	0	1	0	1	0	H9CCNNNCLTMLAR-NUD	SM30E51261AA
	Micron	1	0	0	1	0	MT52L1G32D4PG-107 WT-B	SM30KS9890AA

	PLANARID3 (GPIO_F15)	PLANARID2 (GPIO_F14)	PLANARID1 (GPIO_F13)	PLANARID0 (GPIO_F12)
MP	0	0	0	1
	R1106	R1107	R1108	R1109
	ASM	ASM	ASM'	DY

PLANAR ID: 0001 for SDV
0010 for FVT



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緯創資通

Title			
CPU (CSI2/EMMC)			
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LENOVO Confidential to Wistron CSD

KDS 1ZZCAA24000CC0B
TXC 8Y24080002
Epson Q22FA1280027100

TXC 9H03280012
KDS 1TJF090DJ1A000B
EPSON FC-135R (X1A0001410002)

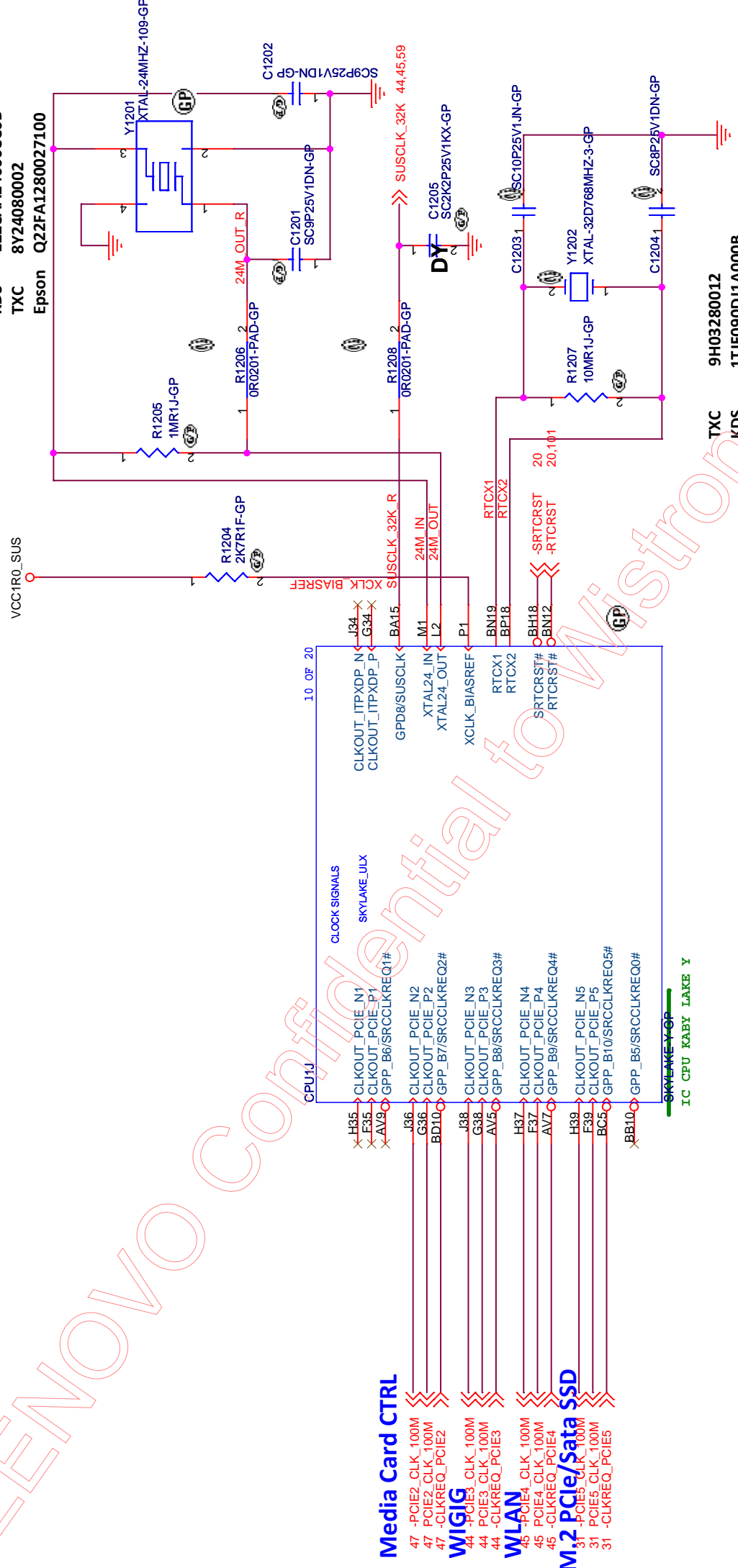
ULX

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CPU(10/16) : CLOCK SIGNALS

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Media Card CTRL

- 47 -PCIE2_CLK_100M
- 47 -PCIE2_CLK_100M
- 47 -CLKREQ_PCIE2

WIGIG

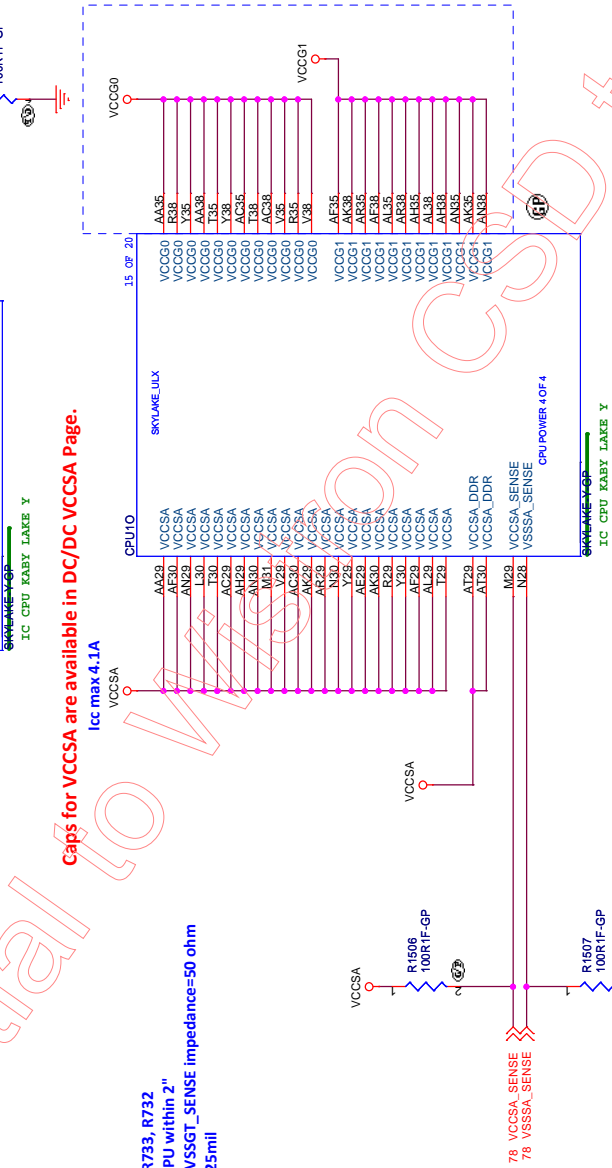
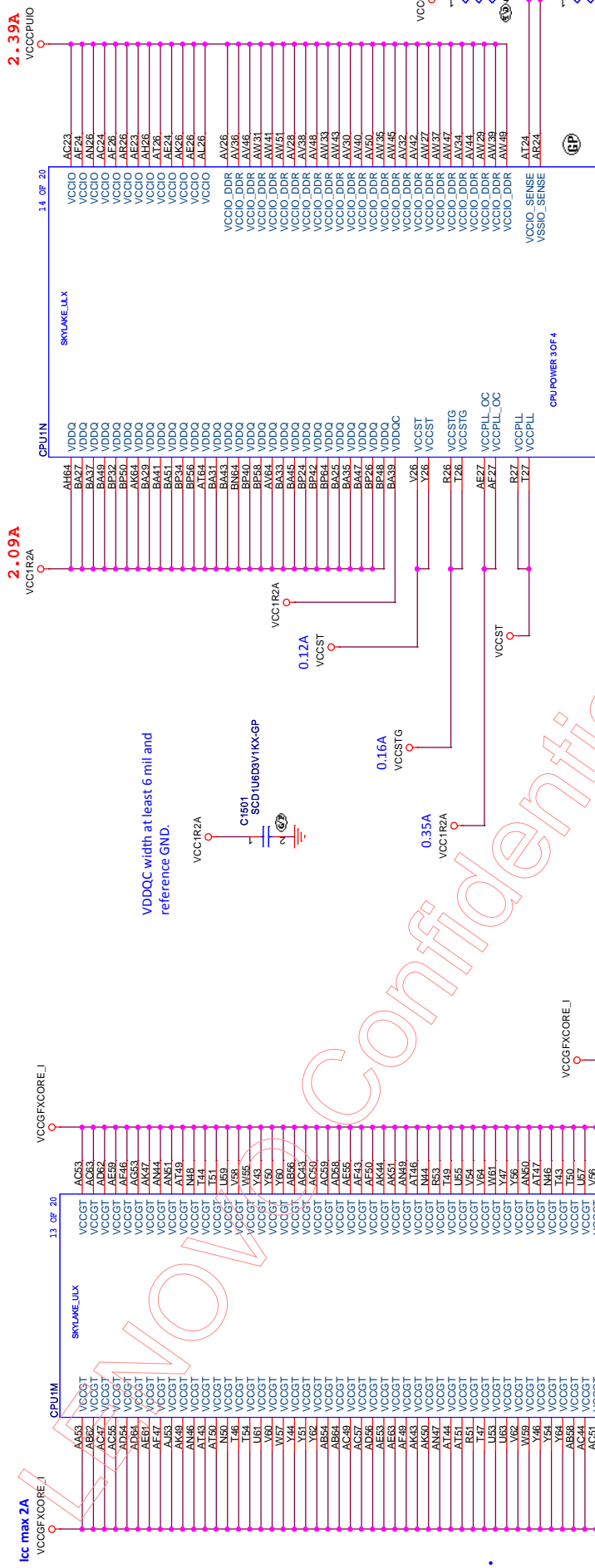
- 44 -PCIE3_CLK_100M
- 44 -PCIE3_CLK_100M
- 44 -CLKREQ_PCIE3

WLAN

- 45 -PCIE4_CLK_100M
- 45 -PCIE4_CLK_100M
- 45 -CLKREQ_PCIE4

SATA

- 31 -PCIE5_CLK_100M
- 31 -PCIE5_CLK_100M
- 31 -CLKREQ_PCIE5



Caps for VCCSA are available in DC/DC VCCSA Page.

lcc max 4.1A

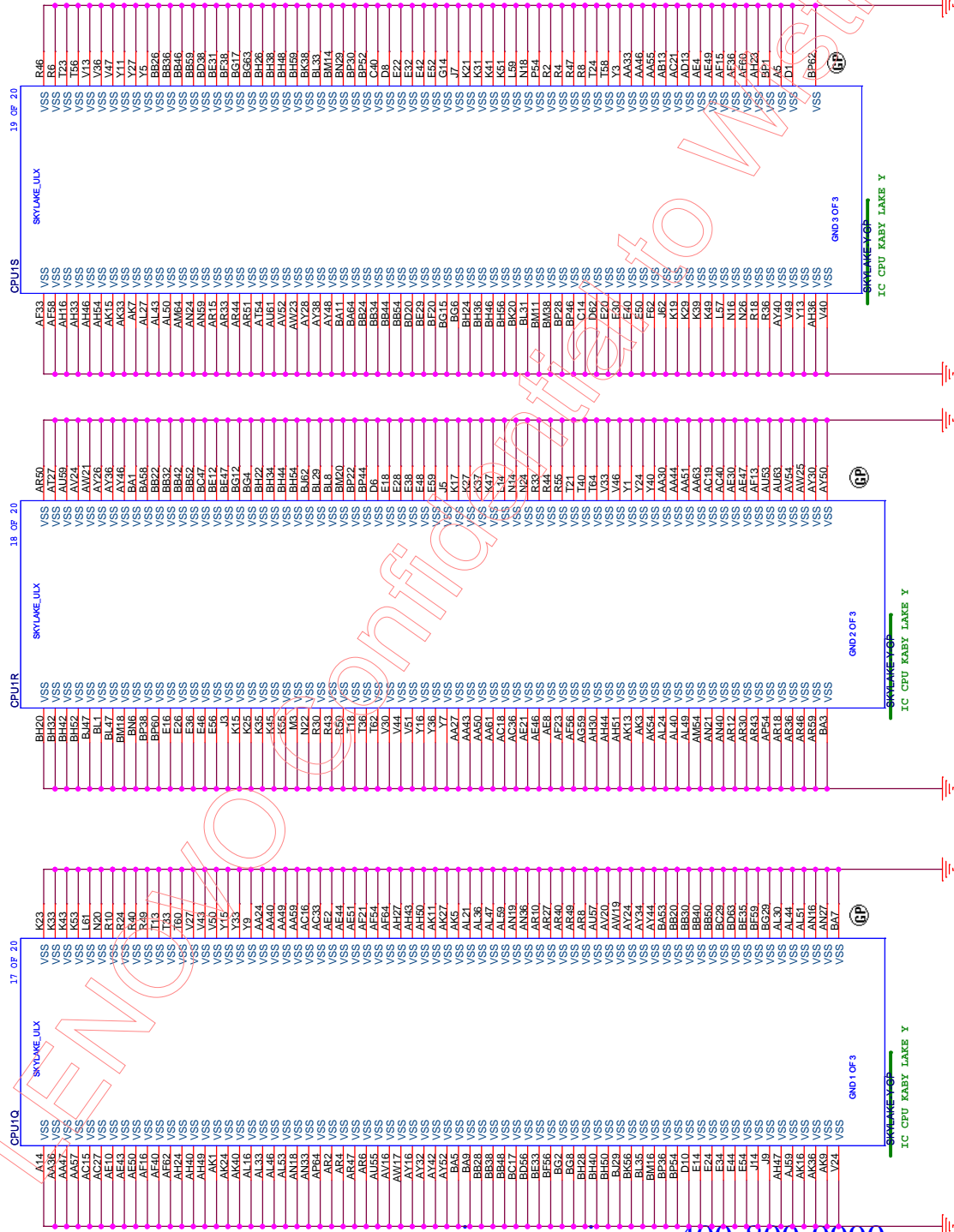
Layout Notes for R733, R732

1. Place close to CPU within 2"

3. Length match < 25mil

Wistron Confidential

Wistron CSD to

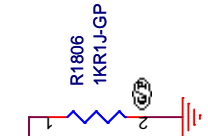


ULX

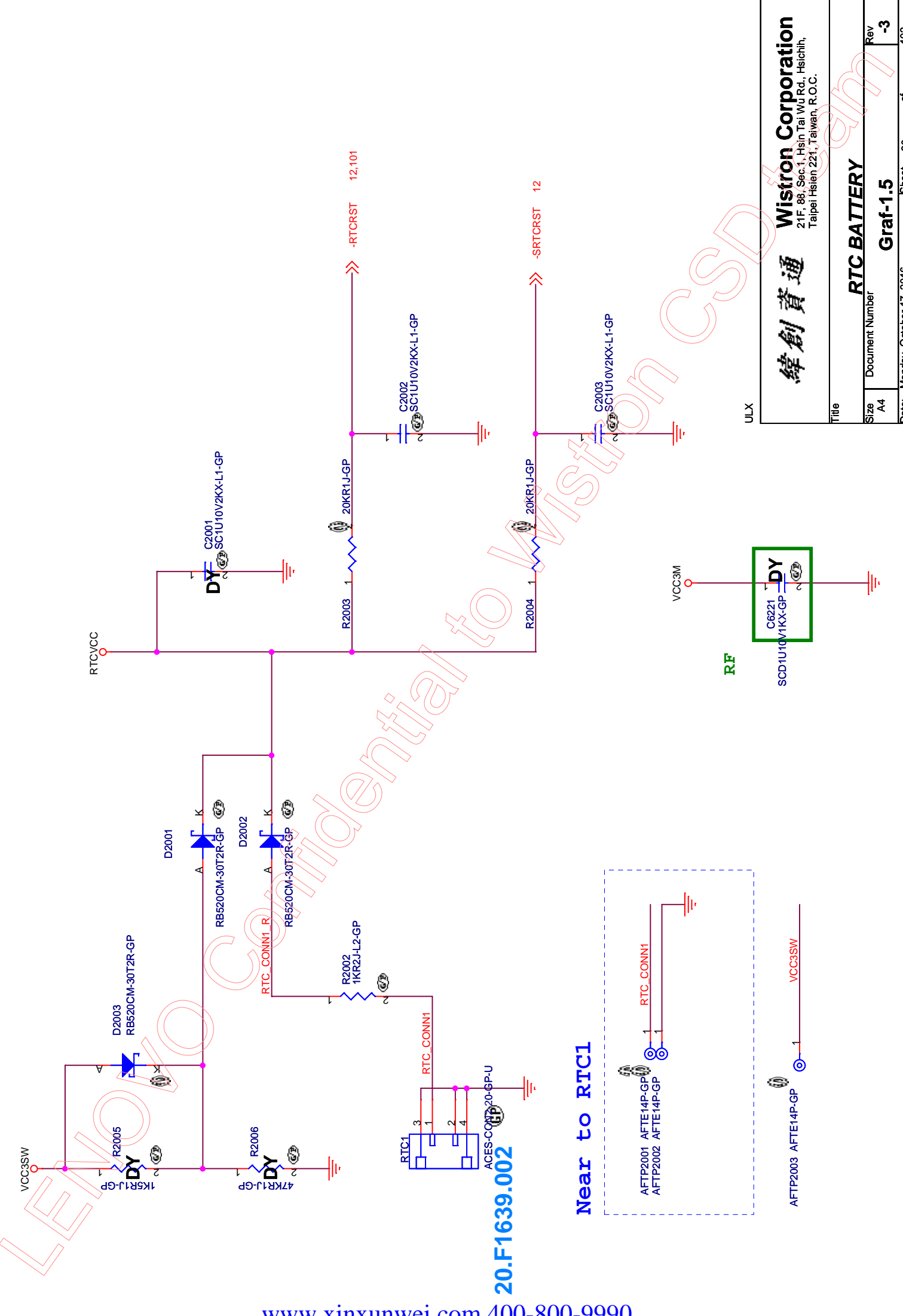
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Rd., Hsinshih,
Tapei (Hsin 22), Taiwan, R.O.C.

Title		CPU(15/16) : GND	
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0: VR DOES NOT SUPPORT SVID

1 : DISABLED
NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

Date: Monday, October 17, 2016



ULX

RF

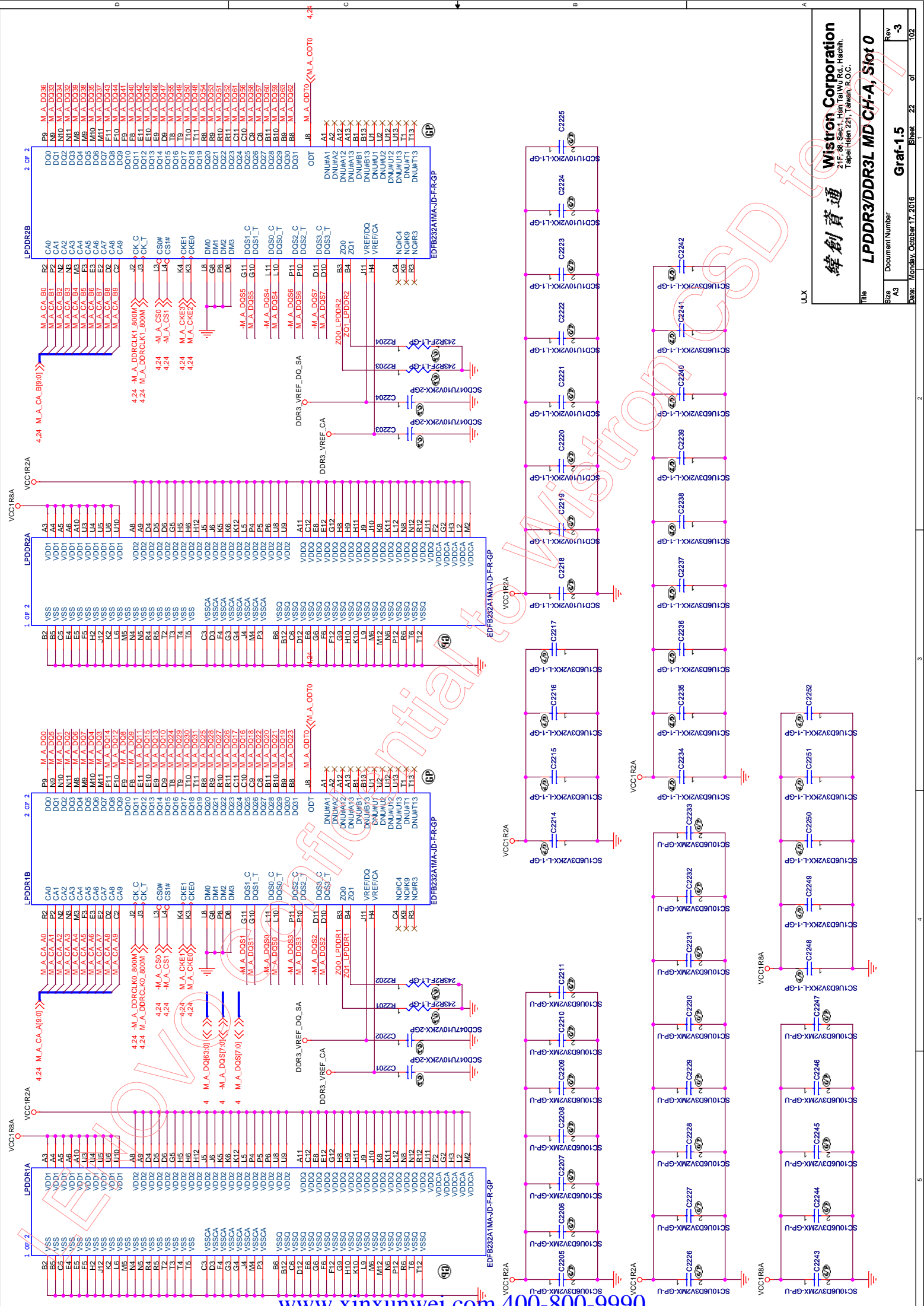
Near to RTC1

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Taipei Hsien 221, Taiwan, R.O.C.

RTC BATTERY

Size	Document Number	Rev
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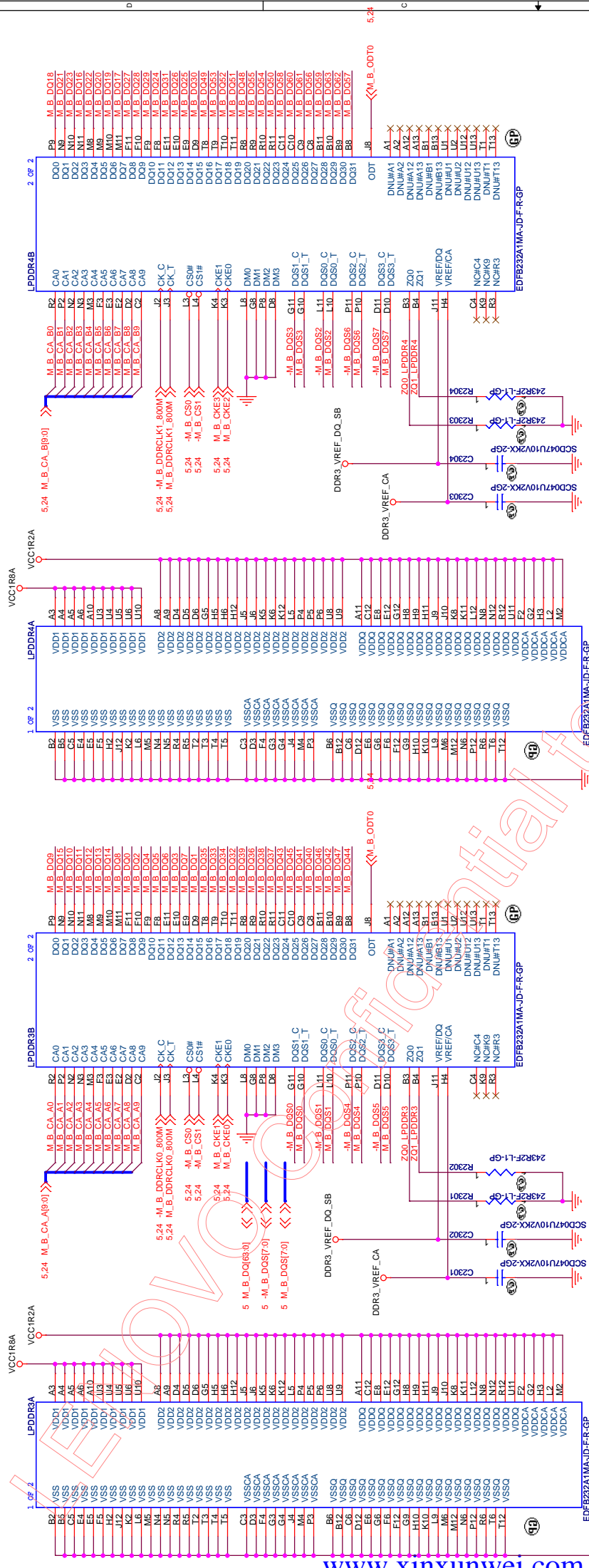
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File		LPDDR3/DDR3L MD CH-A, Slot 0	
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Taippei (New 225), Taiwan, R.O.C.

File

LPDDR3 MD CHANNEL-B (1/2)

Size

A3

Document Number

Grat-1.5

Rev

-3

Date

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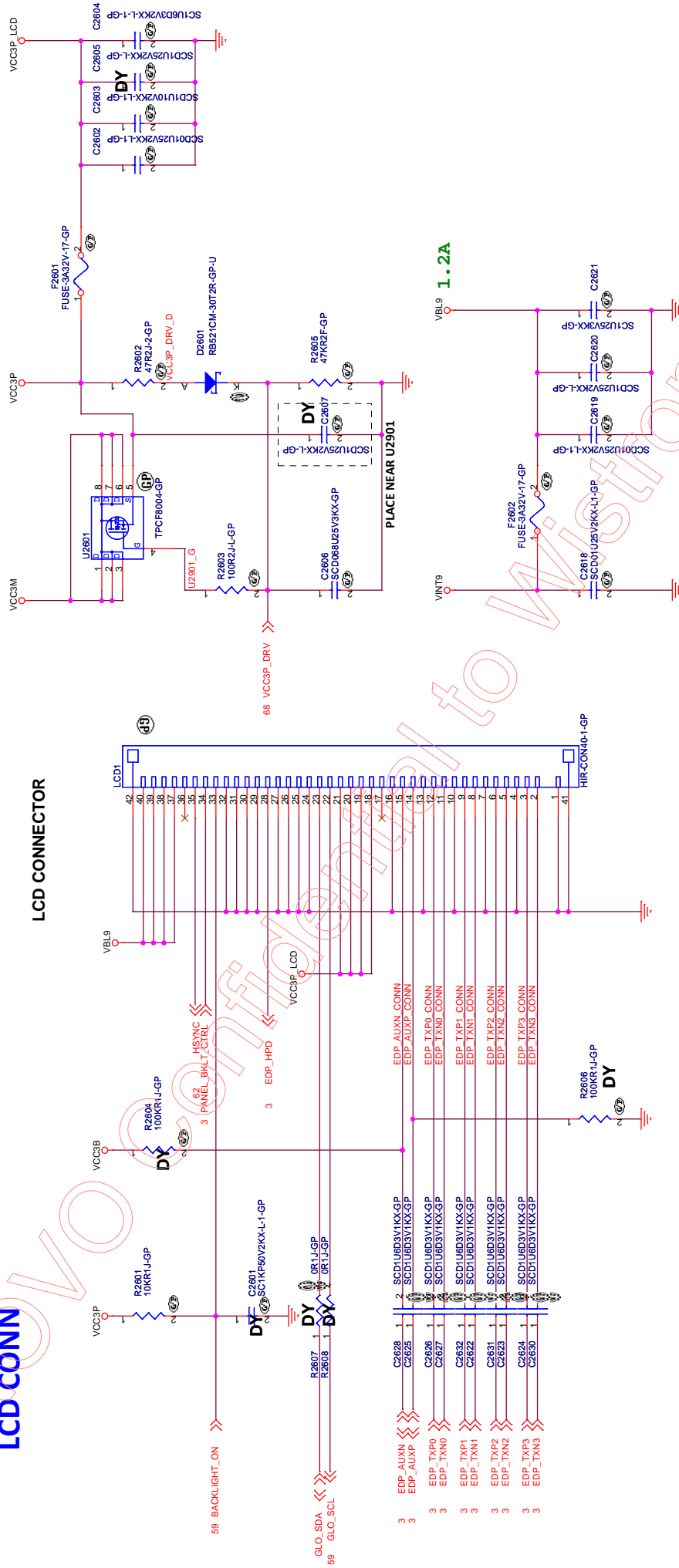
ULX

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		BLANK	
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0.9A

LCD CONN

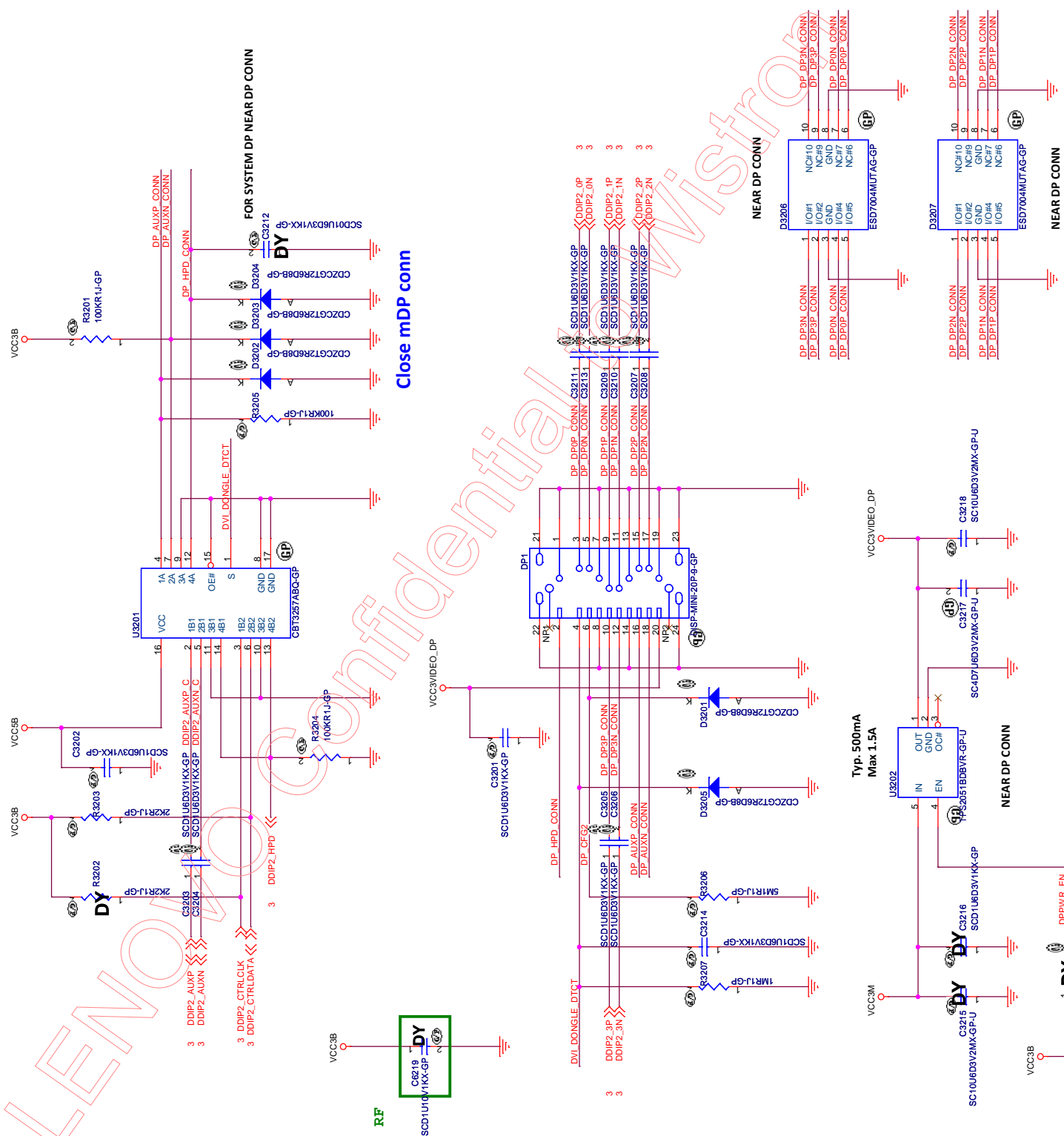
LCD CONNECTOR



VINT9
AFTE14P-GP AFTP806

ULX

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緯創資通	
LCD CONN	
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Priority setting in Automatic Switching Mode

	DDI1_PRIORITY1	DDI1_PRIORITY2	DDI1_PRIORITY_MID
Port1>Port2>Port3(default)	L	L	X
Port1>Port3>Port2	H	L	L
Port3>Port2>Port1	L	H	L
Port3>Port1>Port2	H	H	L
Port2>Port1>Port3	H	L	H
Port2>Port3>Port1	H	H	H

Place CAPS as close as to CPU side

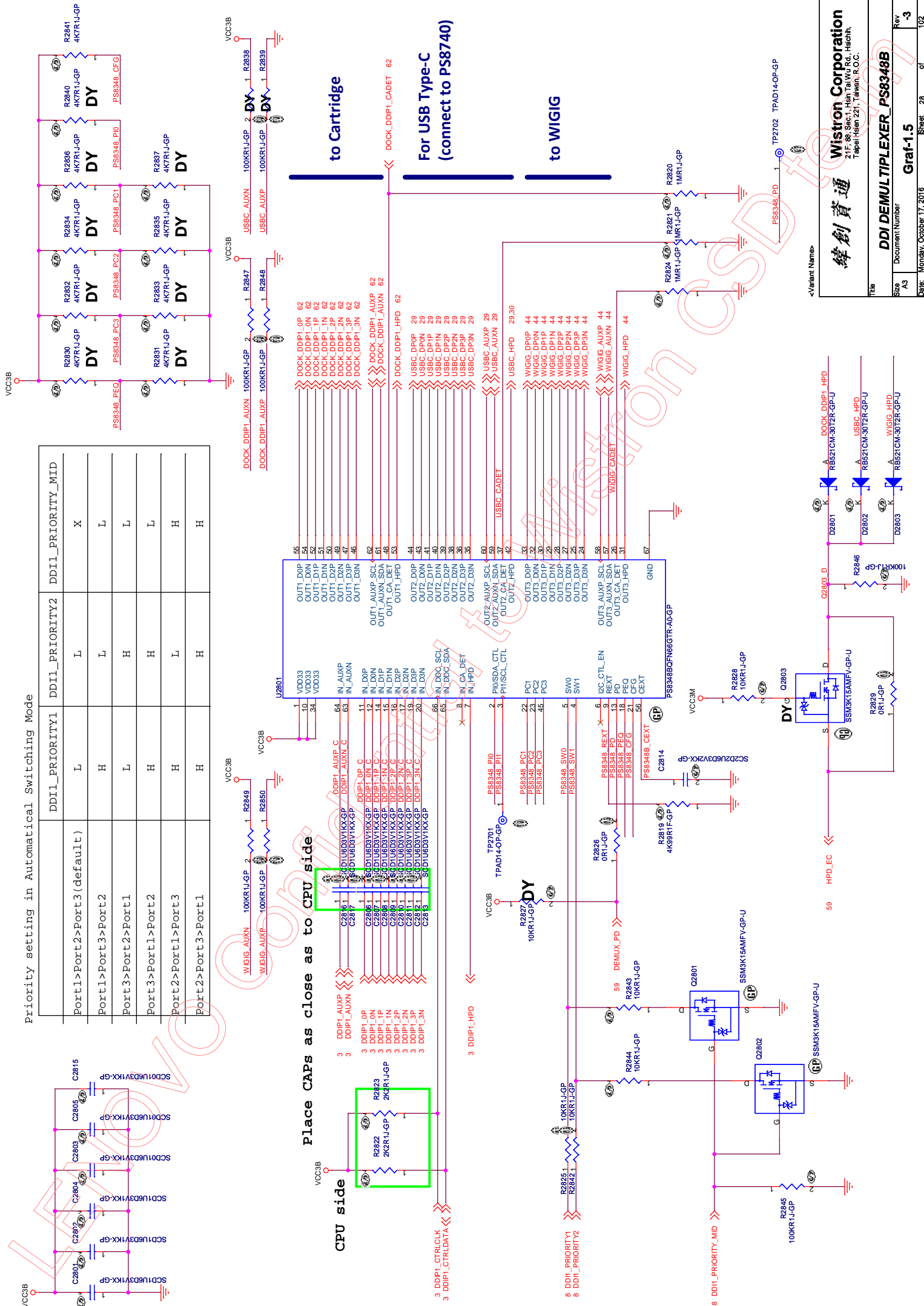
CPU side

to CPU side

to Cartridge

For USB Type-C
(connect to PS8740)

to WIGIG



<Variant Name>

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Tapei (Taiwan), Taiwan, R.O.C.

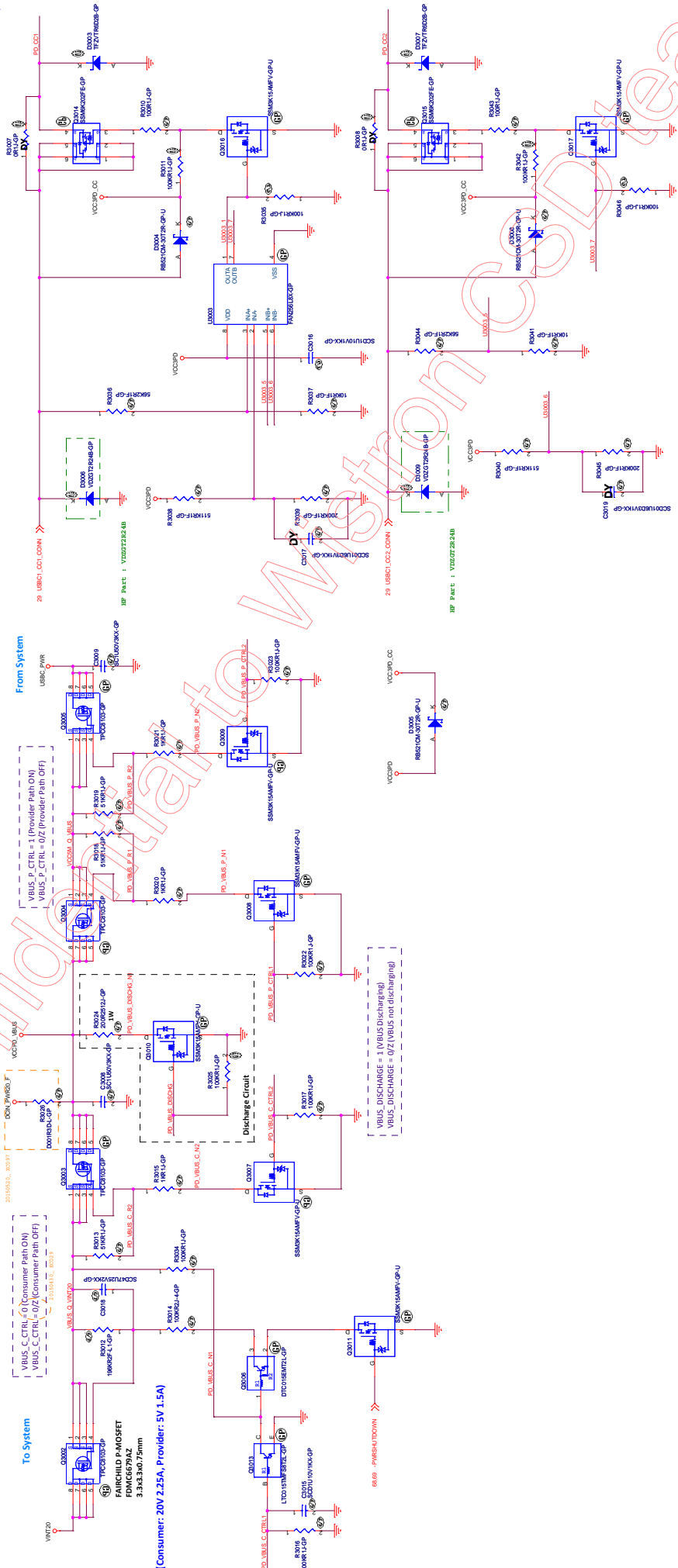
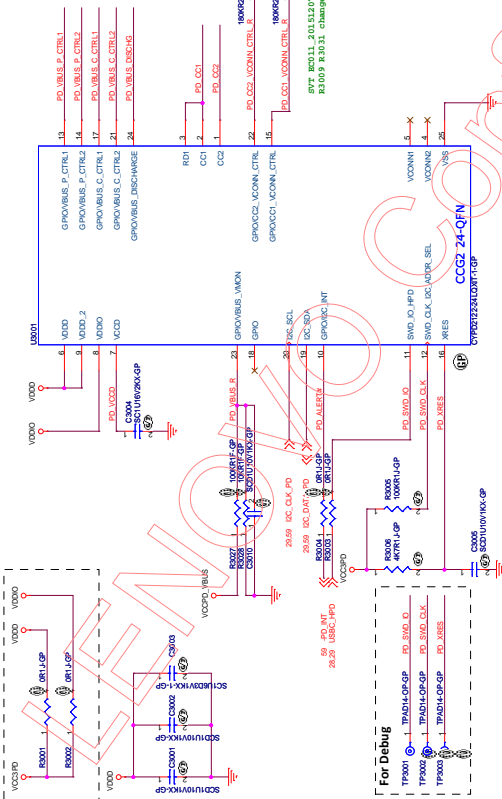
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Size	A3
Document Number	Grat-1.5
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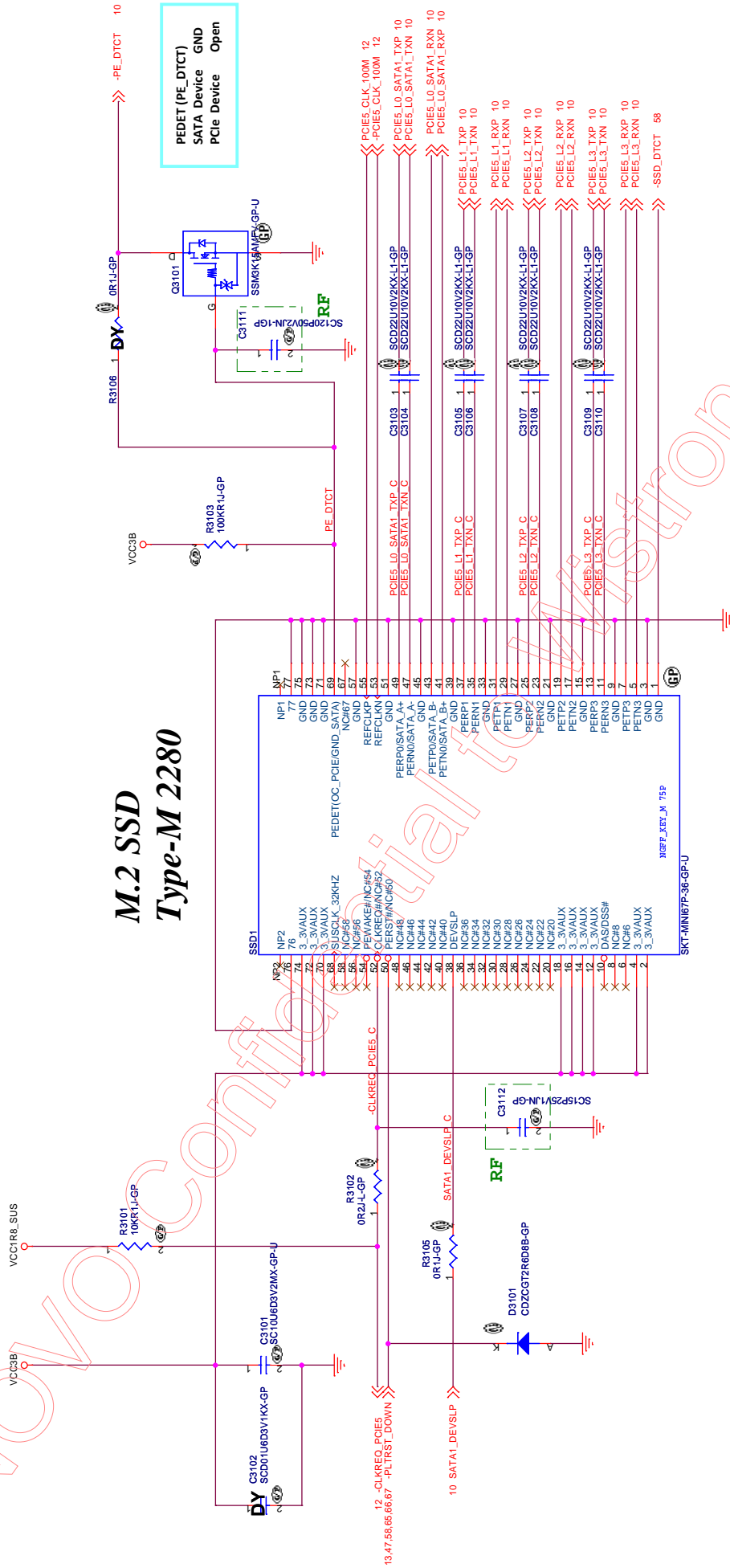
USB PD

Platform	Vendor Name	Vendor P/N	Wistron P/N	Die revision	PD firmware
Grat1	Cypress	CG8584AAT (*)	074.08584.0073	A	ver. 7.1
Grat1.5	Cypress	CYPD02122-24LQX1		B	ver. 8.0

(*) CG8584AAT (CYPD02122-24LQX1 rev.A)



M.2 SSD Type-M 2280



ULX

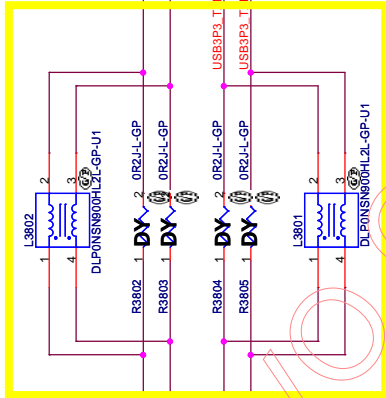
緯創資通
Wistron Corporation
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Taipei (Rien 22), Taiwan, R.O.C.

Title		SSD CONN	
Size	Document Number	Rev	Rev
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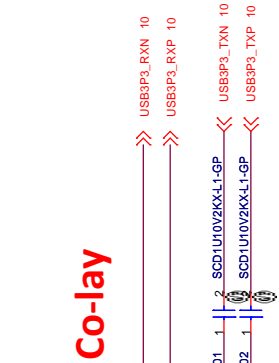
USB 3.0

breadboard

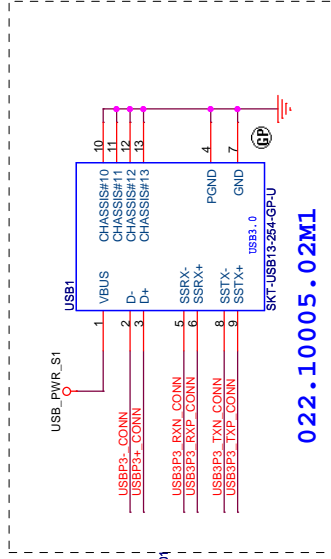
Standard CONN
USB3.0



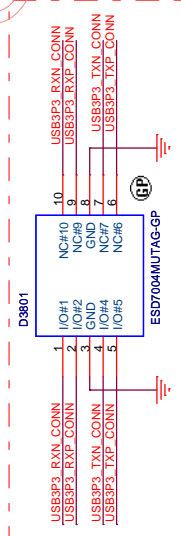
Co-lay



USB3.0



022.10005.02M1



Co-lay

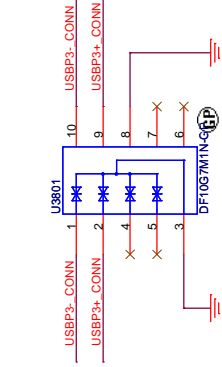
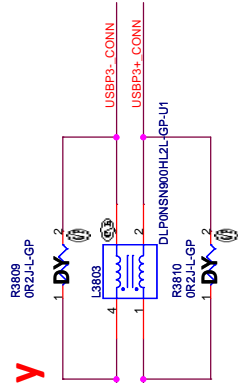
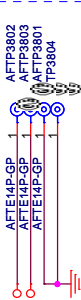


TABLE of TVS DIODE: D3902

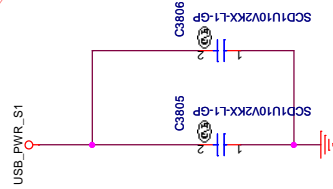
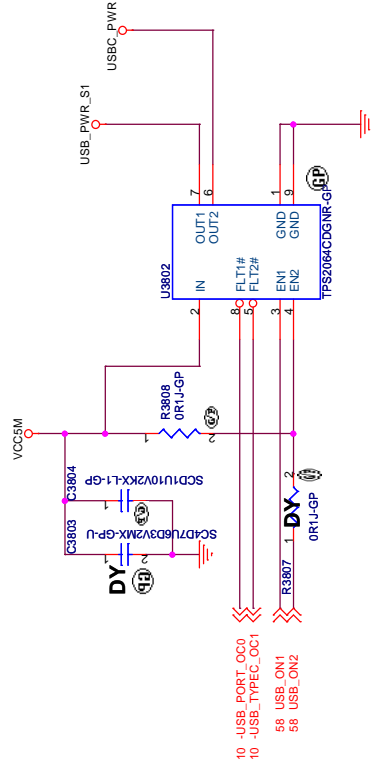
	Vendor	Vendor P/N	Wistron P/N
1st	ON	ESD7004MUTAG	83.07004.0A0
2nd	NXP	PUSB3F96	83.04294.0A0

Near USB3.0 CONN: USB1



WIDE PATTERN(MIN 500mA)
PLACE NEAR USB CONN

USB POWER



Active High
Continuous Current Limit 1.5A

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USB POWER/CONN

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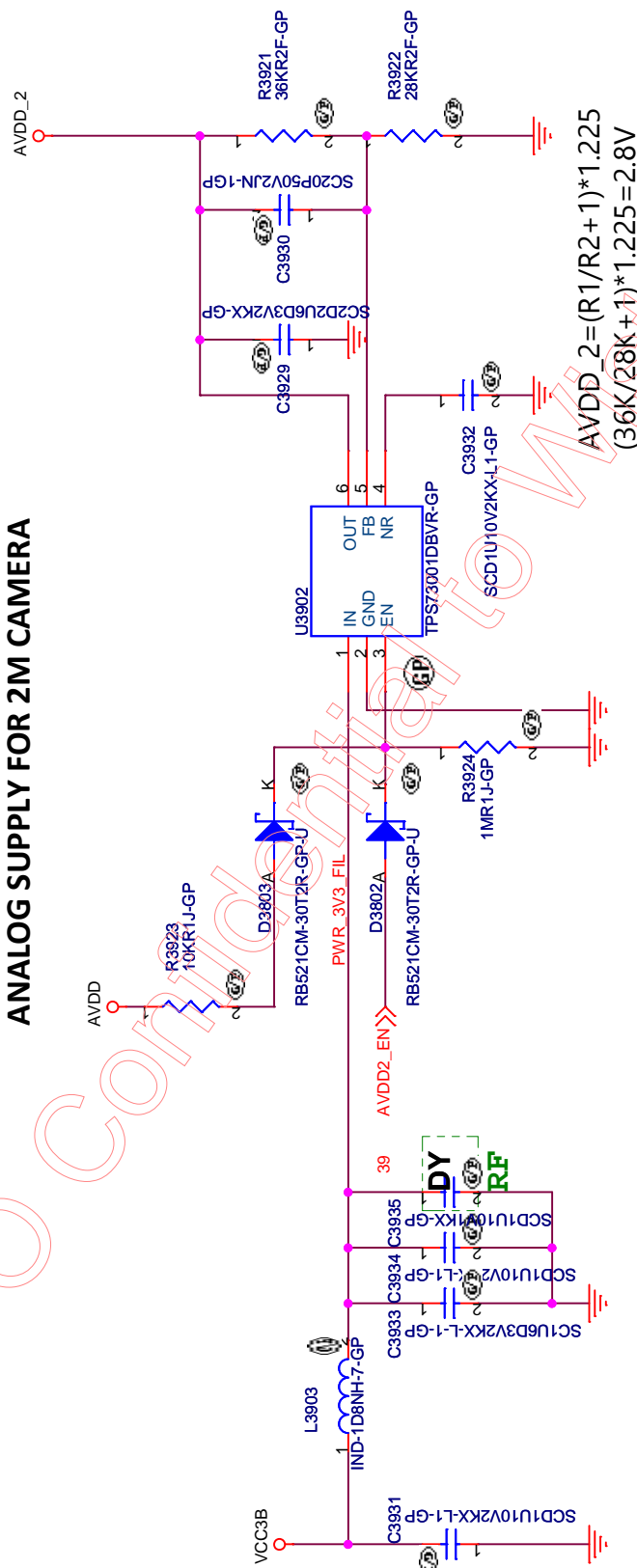
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ANALOG SUPPLY FOR 2M CAMERA



$$AVDD_2 = (R1/R2 + 1) * 1.225$$

$$(36K/28K + 1) * 1.225 = 2.8V$$

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Title

Camera AVDD 2

Size	Document Number
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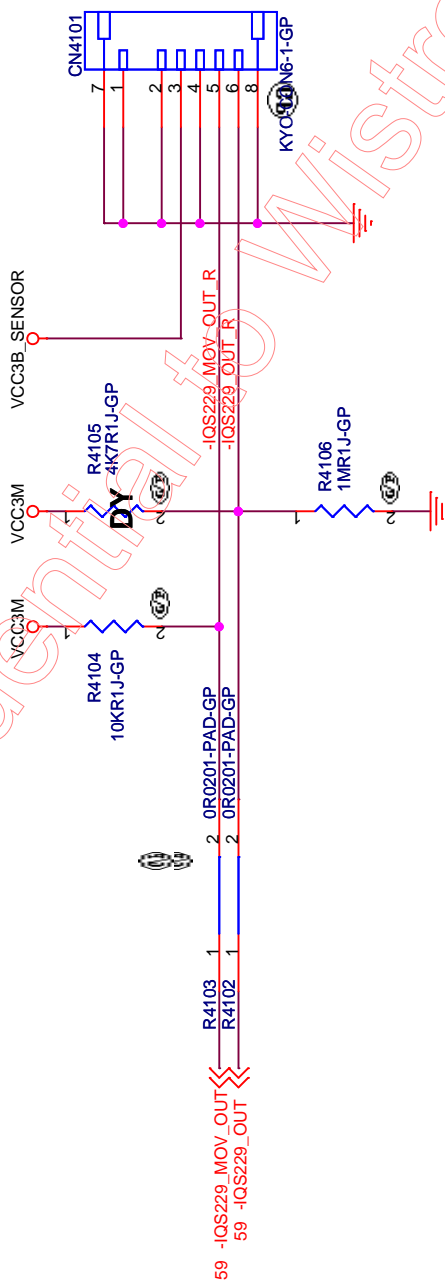
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20150327 EC058

- Change signal name
- Add 10K pull-up to VCC3M on -OUT
- Add 1M pull-down to GND on -MOV_OUT

P-Sensor (IQS229)

P-sensor CONN: 020.K0059.0006



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Title
P-SENSOR

Size
A4

Document Number
Graf-1.5

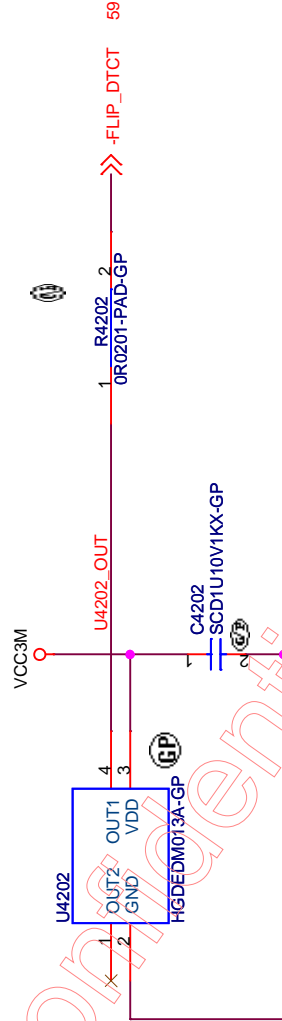
Rev
-3

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Hall Sensor

For Flip mode



ULX

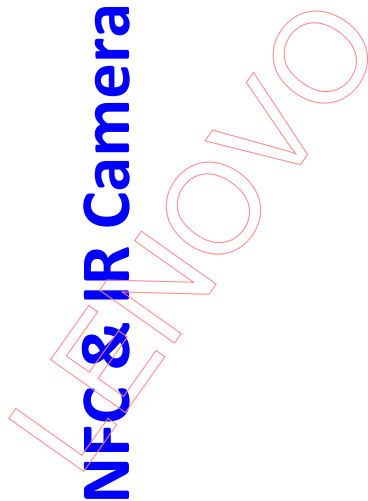
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Hall Sensor

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NFC & IR Camera



X-71m

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NFC & IR CAMERA

Document Number

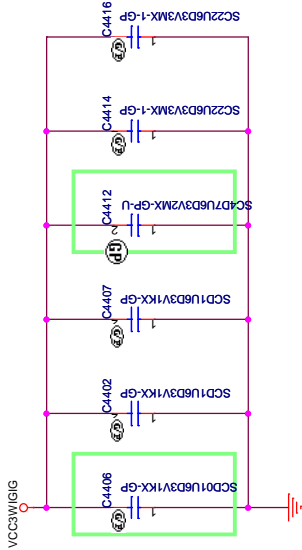
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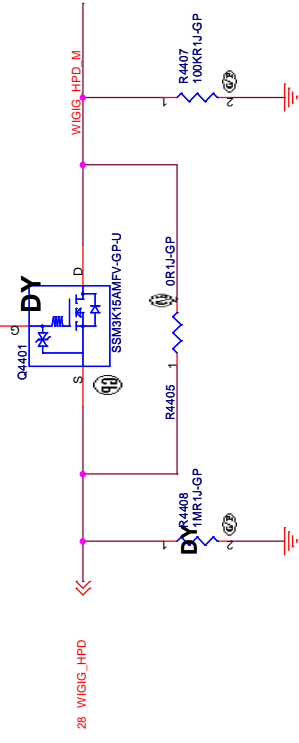
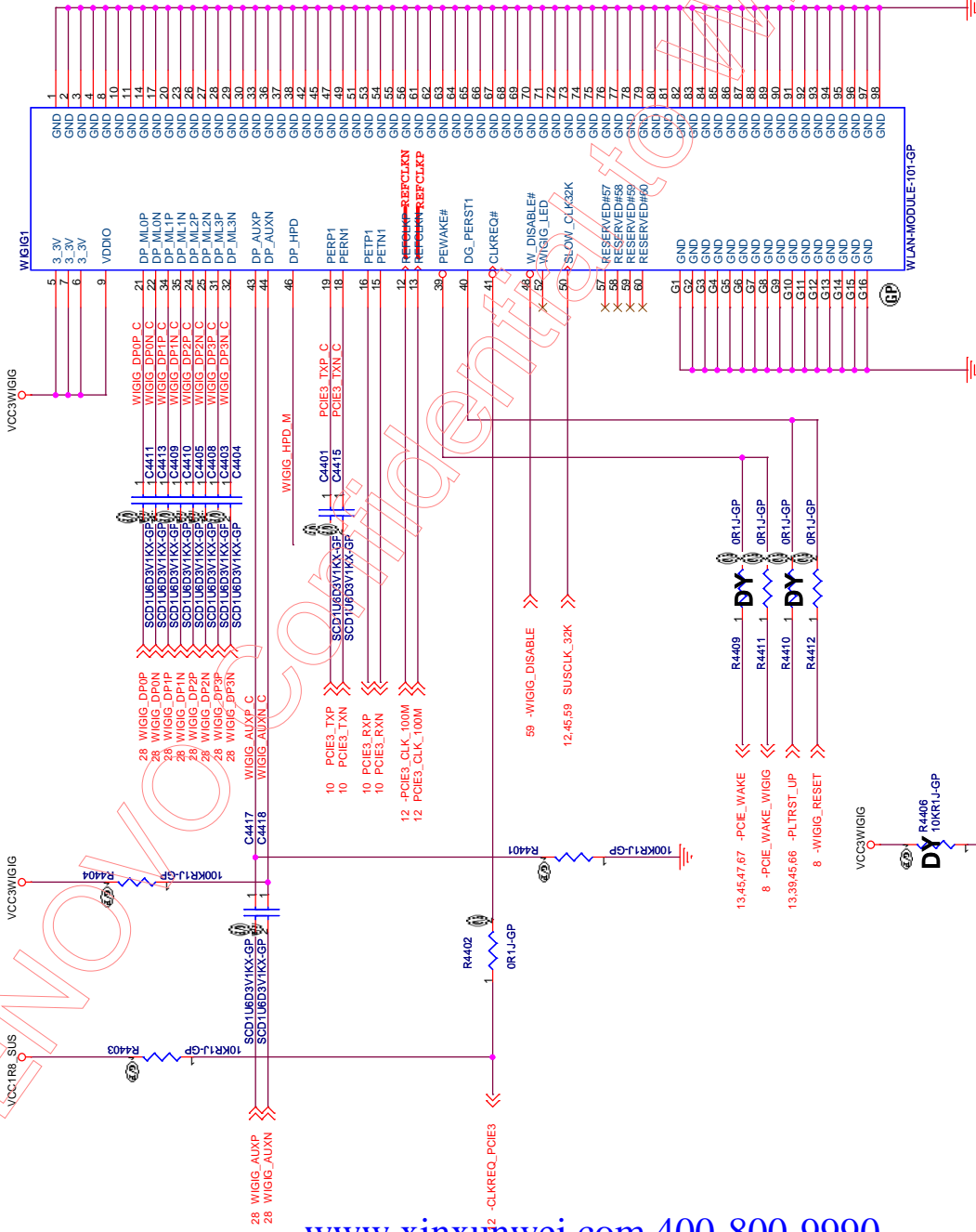
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Intel Request for Test Pad Adding 5/28

- PCie CLK
- PCie CLKREQ
- WAKE
- PERST
- W_Disable
- PCie lanes
- DP AUX
- HPD
- one DP Lanes
- SUSCLK



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Wistron Corporation		Rev	-3
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Taper (Rev. 22), Taiwan, R.O.C.		Size	A3
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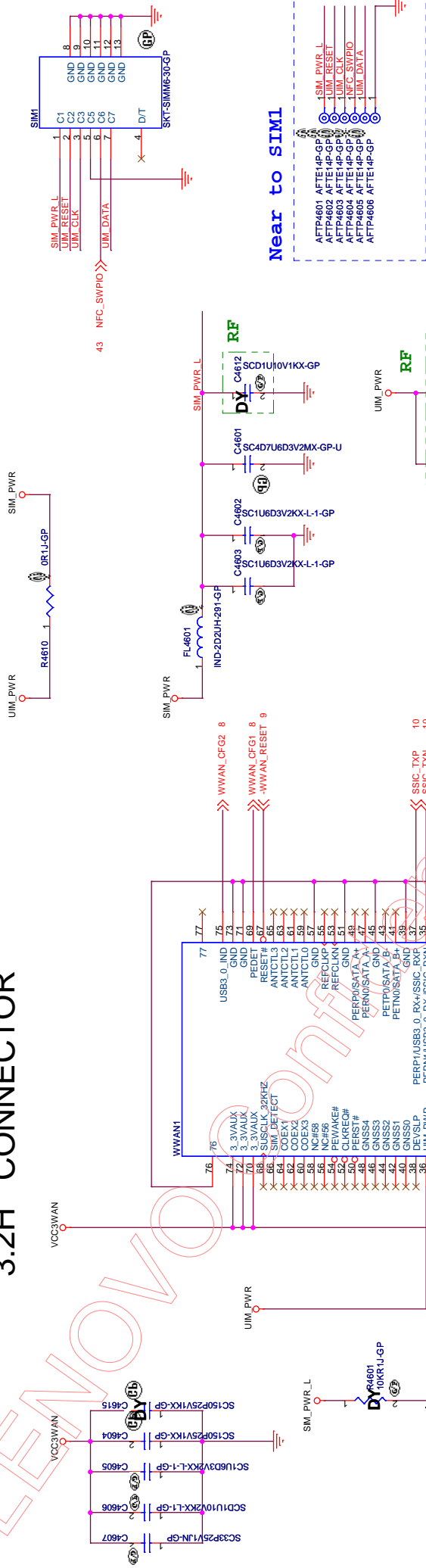
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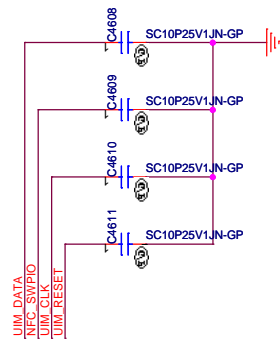
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TYPE-B M.2 CARD FOR WWAN 3.2H CONNECTOR

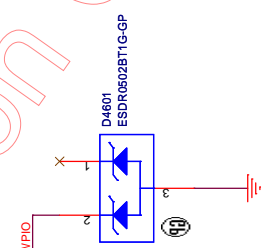
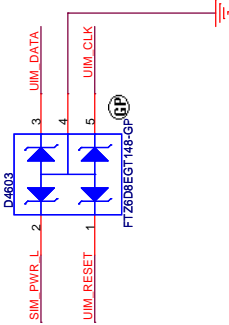
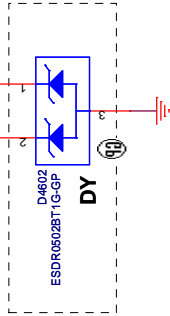
SIM CONN



EMC solution



PLACE NEAR WWAN1

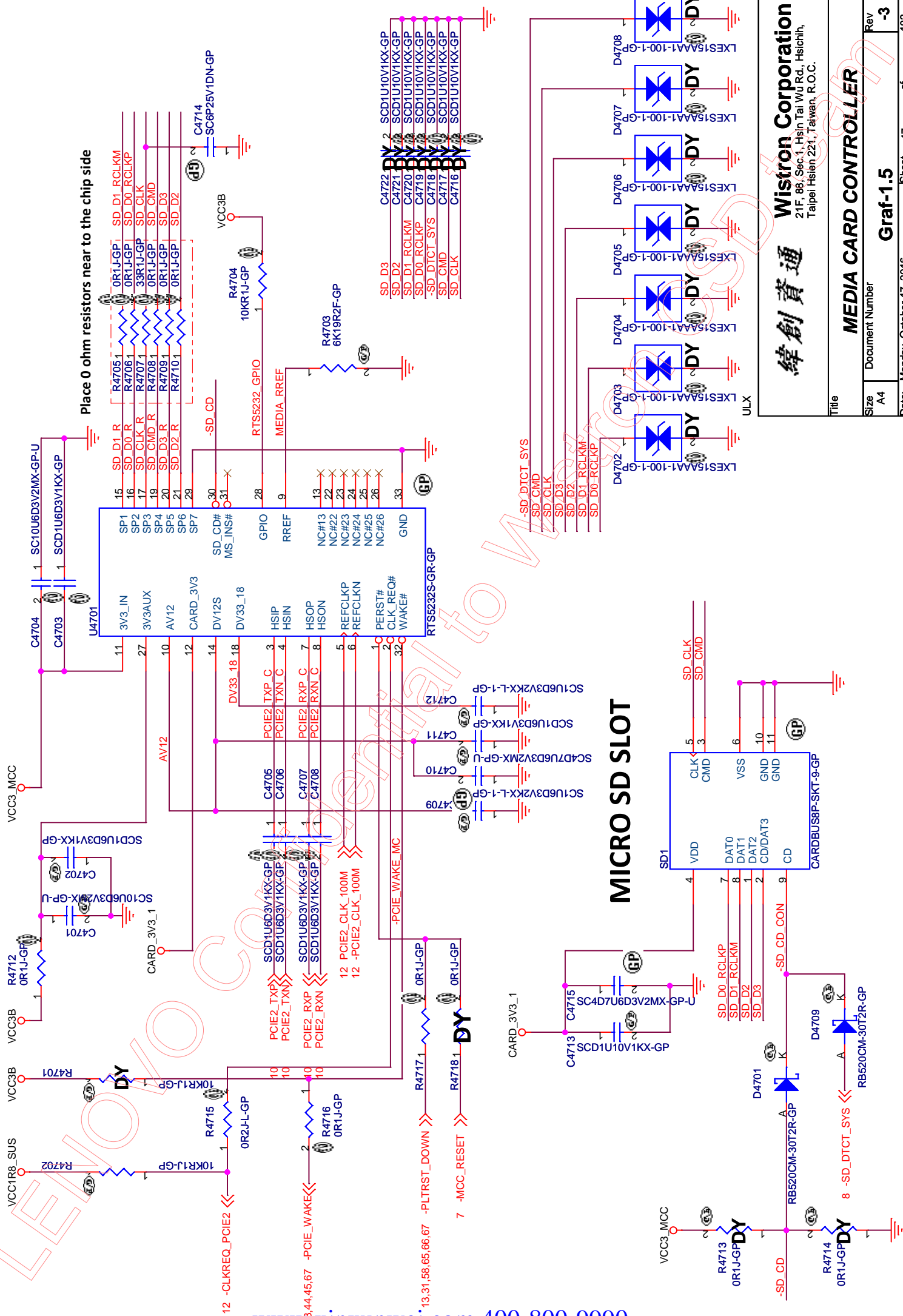


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Place 0 ohm resistors near to the chip side



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Media Card Controller

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<Variant Name>

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Title
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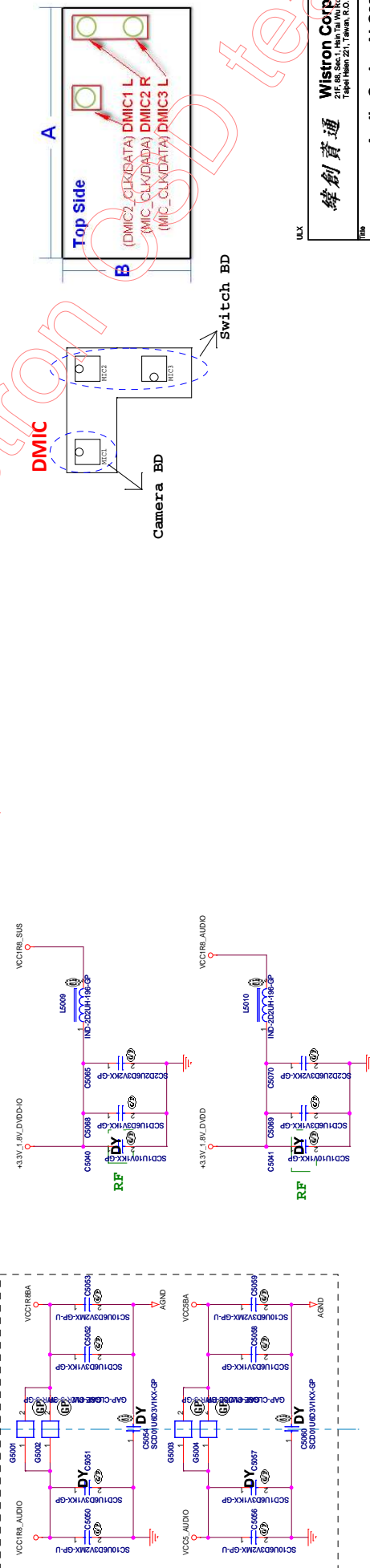
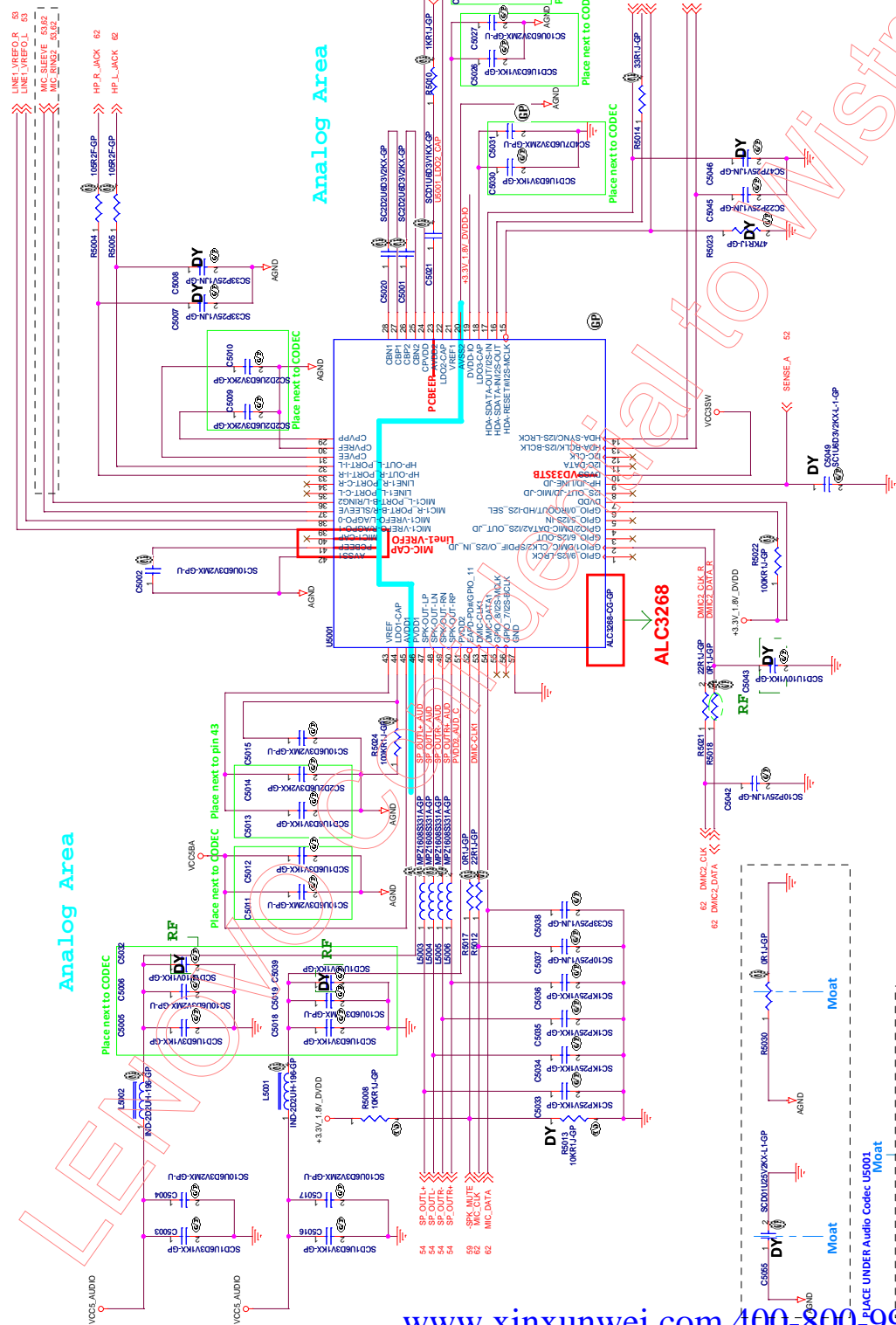
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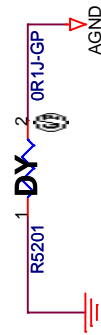
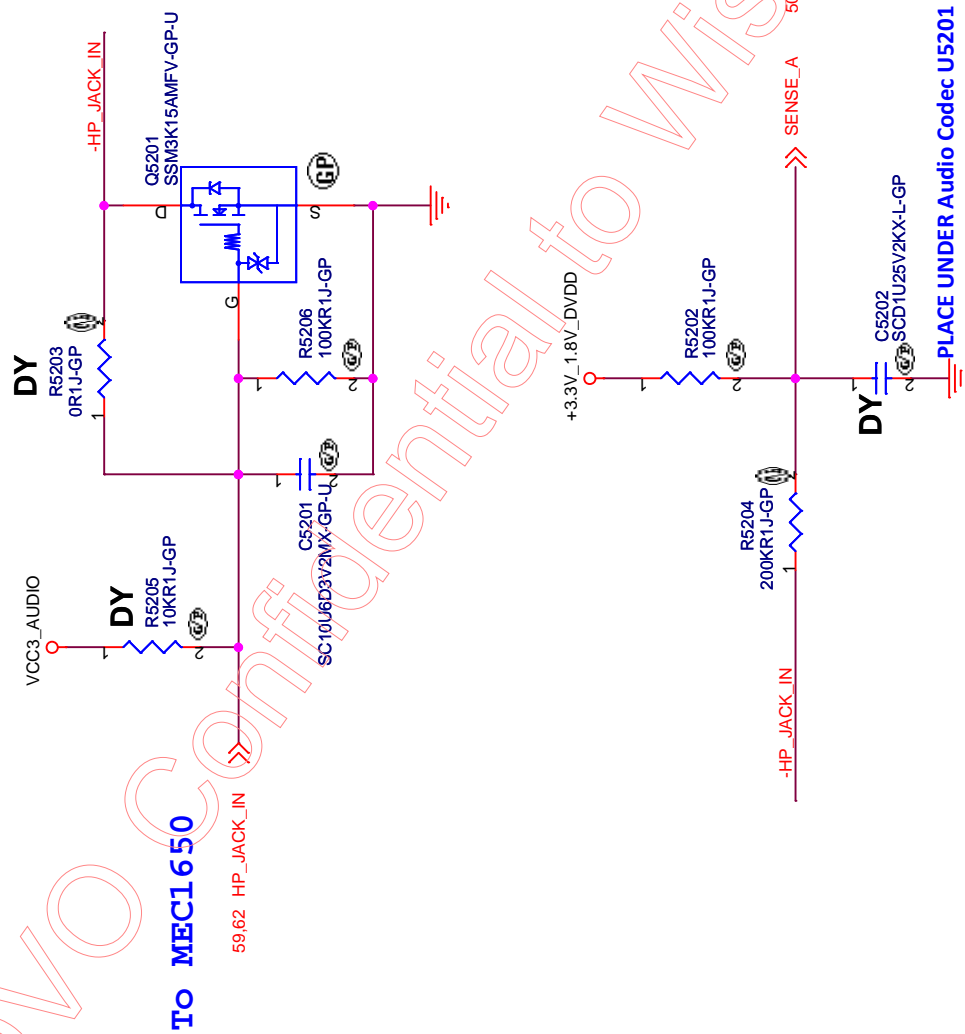
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Title		
Cartridge Connector		
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wide shape for RING2 and SLEEVE
Sleeve/ Ring2 trace width >40mil.
Added 2 via when those two trace change layer for reducing impedance.



For Audio Jack Global Headset Detect Delay Circuit



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Title

AUDIO JACK SENSE

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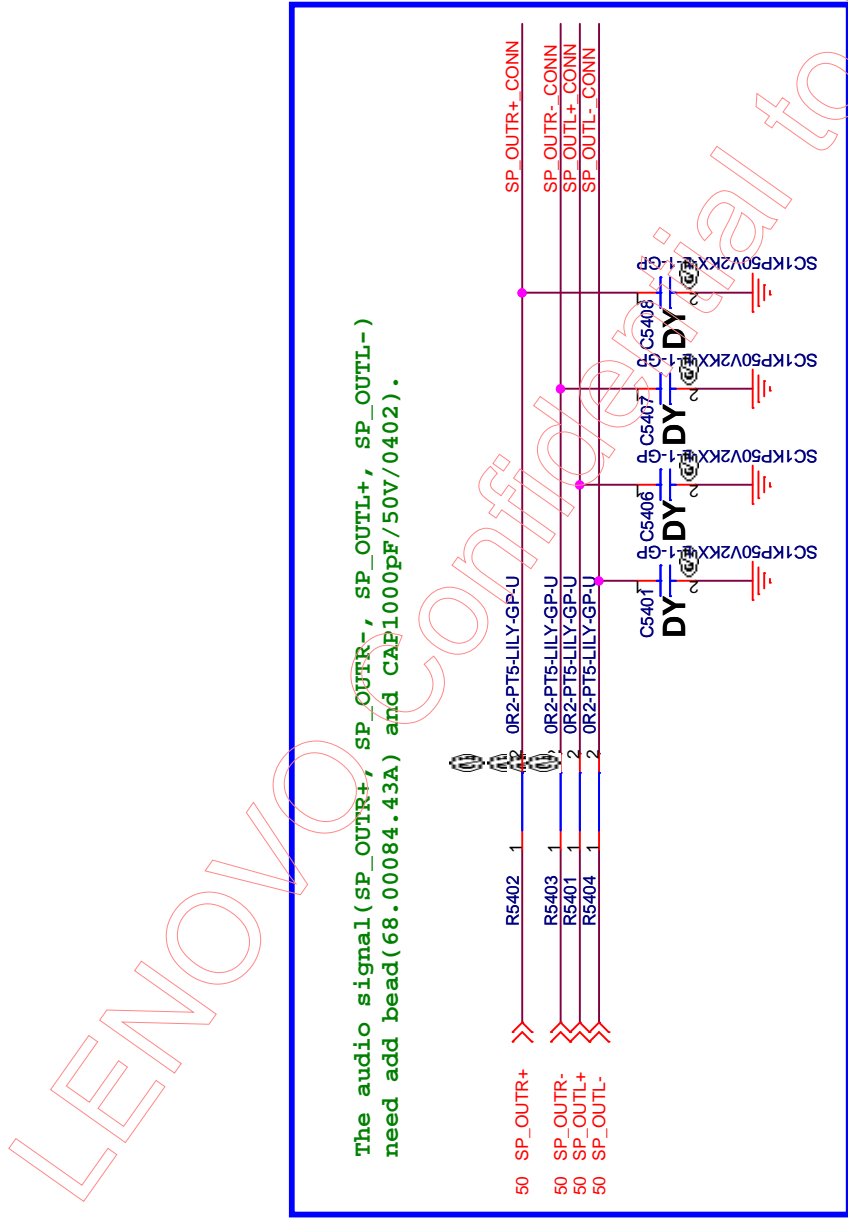
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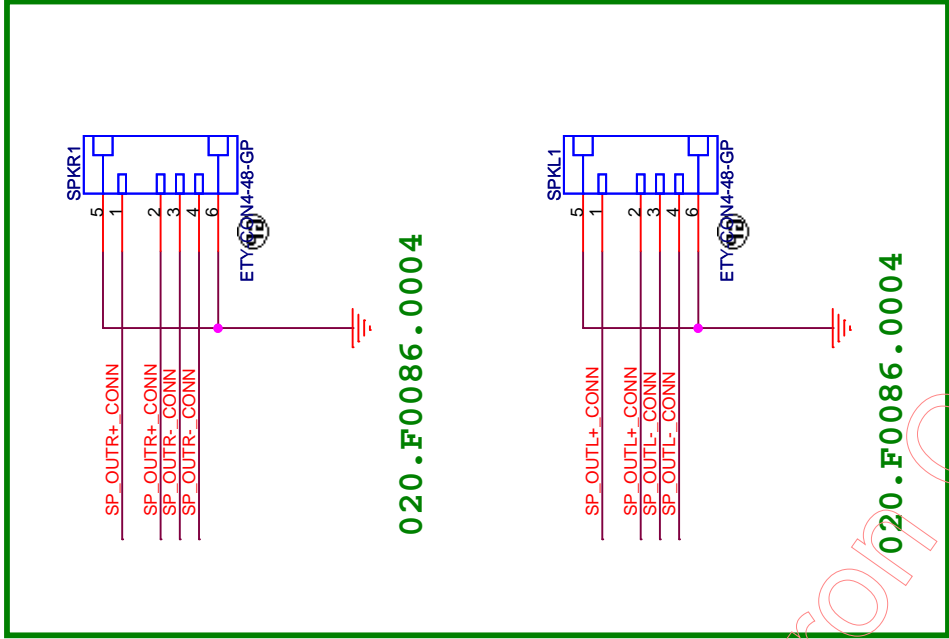
Rev

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SPK L+ L R+ R trace width
 Speaker 4 ohm ==> 40 mils
 Speaker 8 ohm ==> 20 mils

Speaker Connector



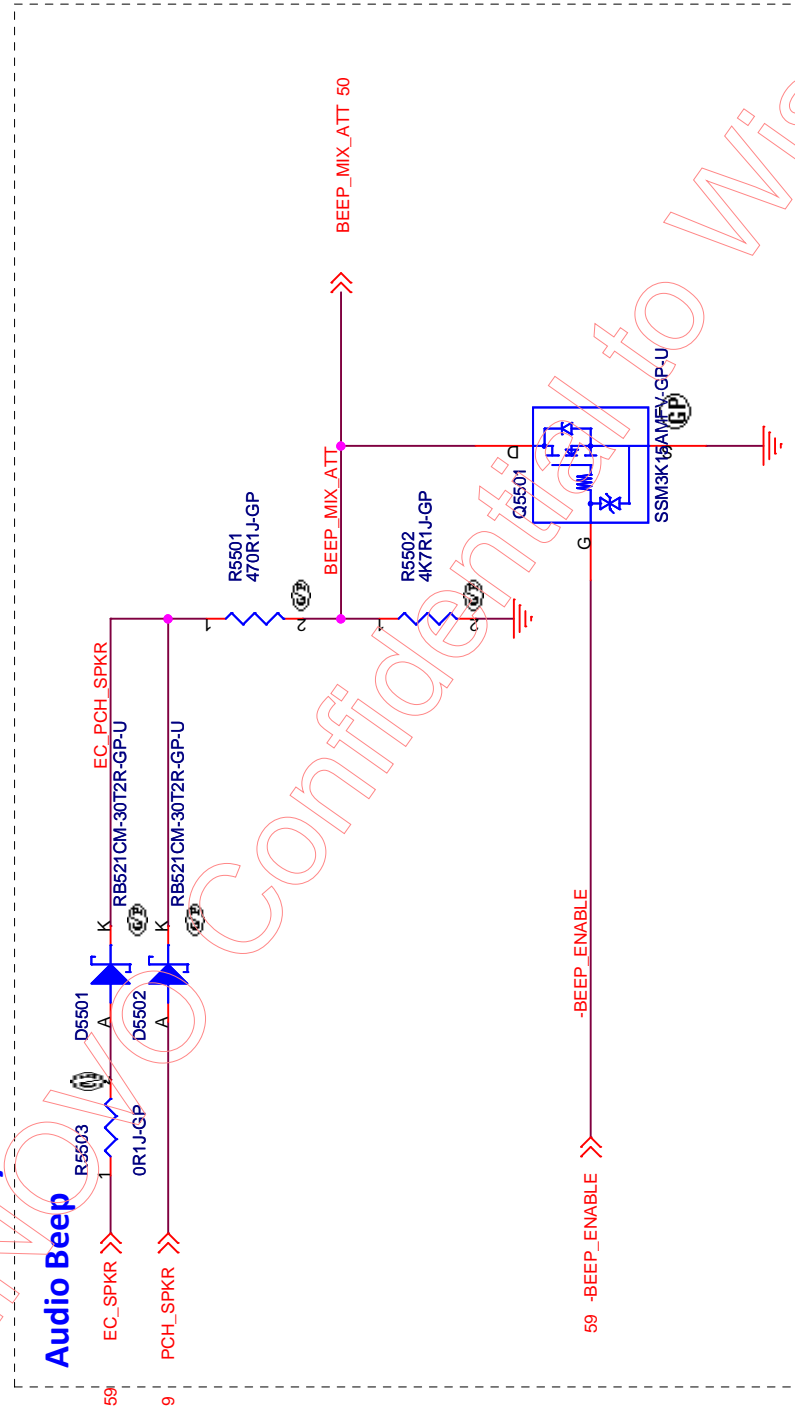
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AUDIO SPEAKER	
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Place near by codec

Audio Beep



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AUDIO BEEP

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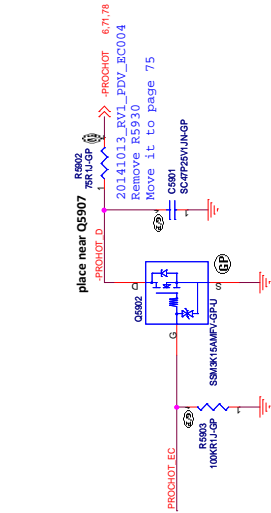
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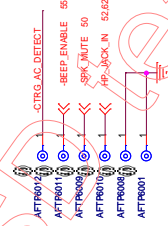
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	Enable	Disable
R5818	22_5%	0_5%
R5819	22_5%	0_5%
R420(?)	NO_ASM	ASM

20150313 under checking



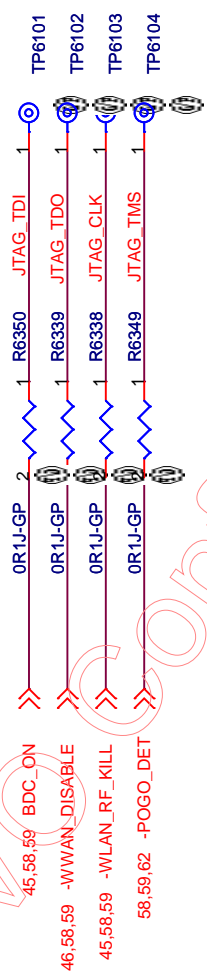
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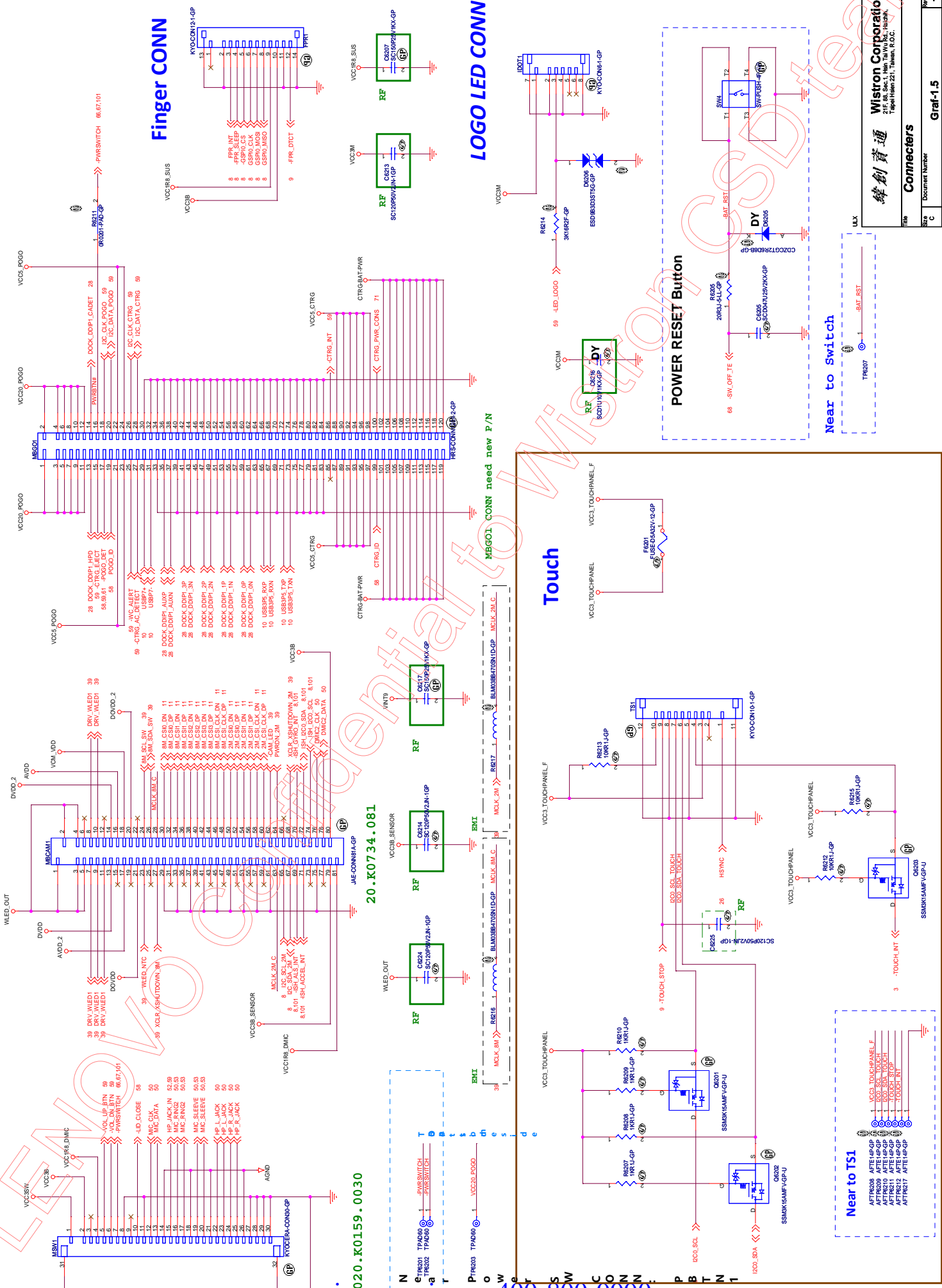
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To Switch BD

To Camera BD

To Pogo BD



Near to TS1

Near to Switch

POWER RESET Button

Touch

LOGO LED CONN

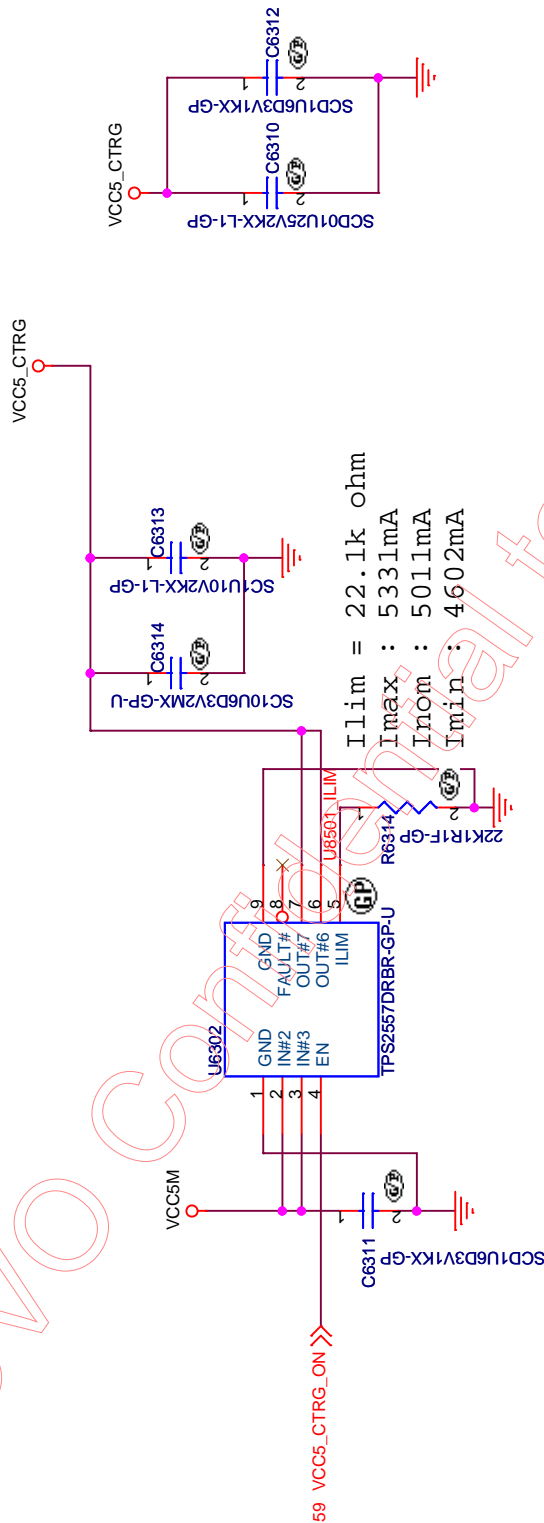
Finger CONN

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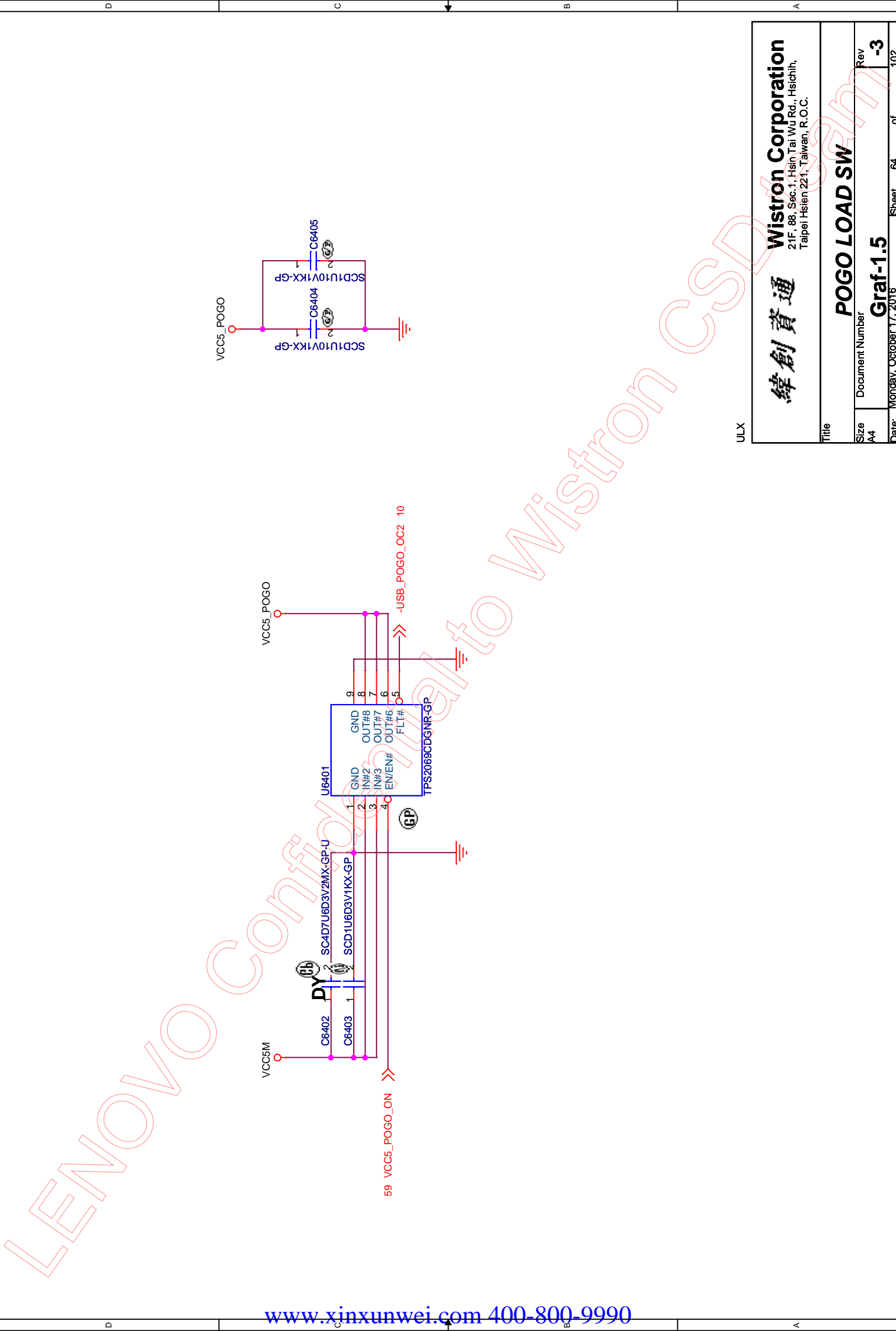
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CTRГ LOAD SW			
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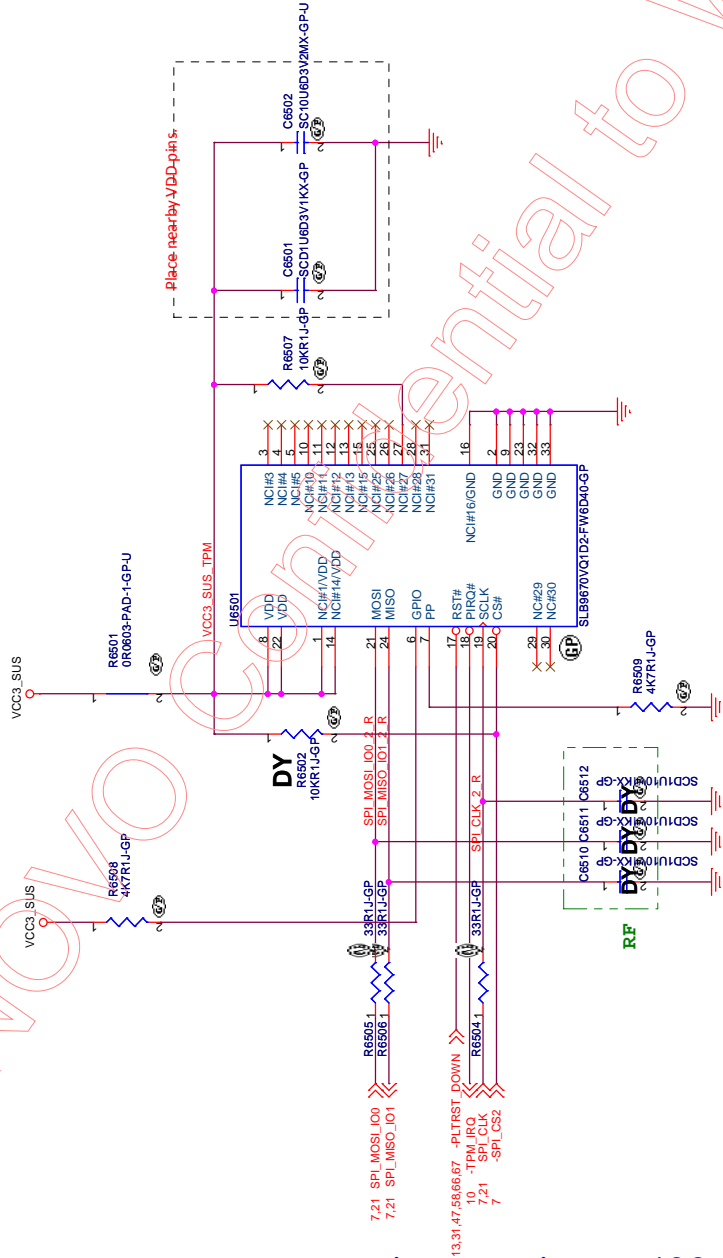
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POGO LOAD SW

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TABLE

Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ1.2 FW6.40	ST Micro ST33HTPM2E3AAD8	Nuvoton NPCT650LB1YX
1	VDD	VDD	NC	VSB
2	GND	GND	GND	NC
3	GPIO	NC	NC	GPX/GPIO2
4	GPIO	NC	PP	PP
5	NC	NC	NC	TEST
6	VNC/GPIO	GPIO	NC	GPIO3
7	GPIO/VDD	PP	GPIO	NC
8	VDD	VDD	NC	VDD
1	GND	GND	NC	GND
2	VNC	NC	NC	NC
3	NC	NC	NC	NC
4	NC	NC	NC	Reserved
5	VNC/GPIO	NC	NC	GPIO4
6	VDD	NC	NC	VDD
7	NC	NC	NC	DNC
8	GND	NC	NC	GND
17	SPI_RST#	RST#	SPI_RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	SPI_IRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	CS#	SPI_CS#	SCS#
21	MOSI	MOSI	MOSI	MOSI
22	VDD	VDD	VPS	VDD
23	GND	NC	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	(SERIRQ)
27	NC	NC	NC	DNC
28	NC	NC	NC	GPIO0
29	VNC/GPIO	NC	NC	GPIO1
30	VNC/GPIO	NC	NC	NC
31	VNC	NC	NC	NC
32	GND	GND	NC	GND



Pin20: CS, need to check with Intel
Pin18: IRQ, need to check with Intel
Pin6:GPIO, please add 4.7k ohm connected to VCC3_SUS
Pin7:PP, please add 4.7k ohm connected to GND

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Title

TPM

Size A3

Document Number

Graf-1.5

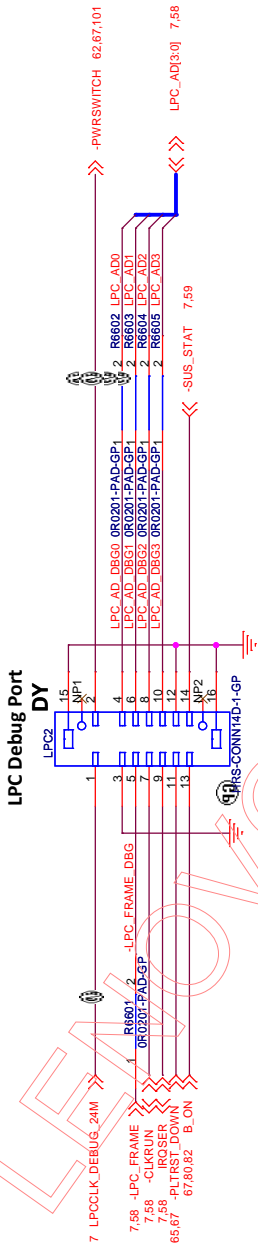
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LPC Debug Port

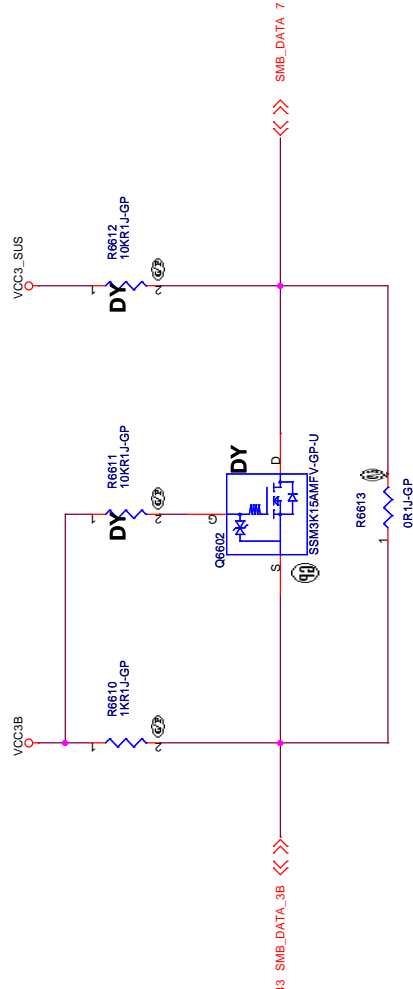
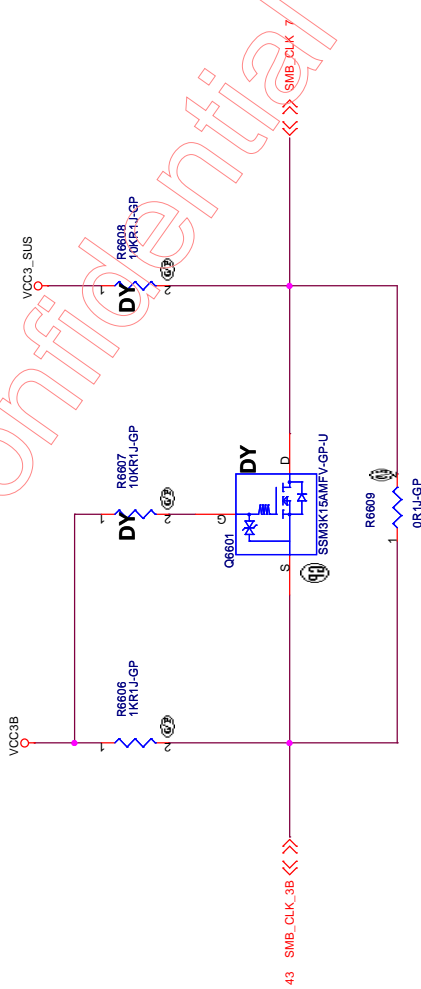


LPC1 Place under WWAN slot

TABLE

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DB1	ASM	NO_ASM
R6614-R6620	ASM	NO_ASM

LOGIC
breadboard

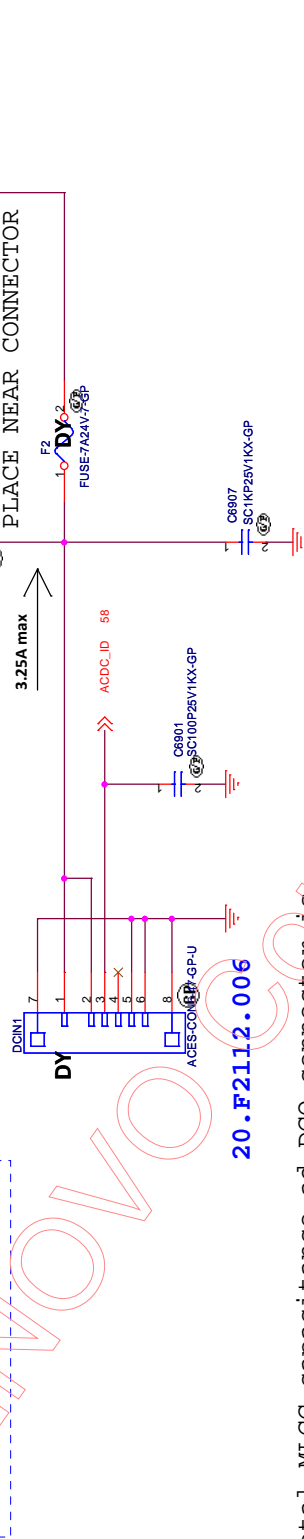
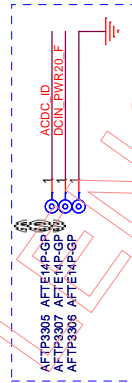


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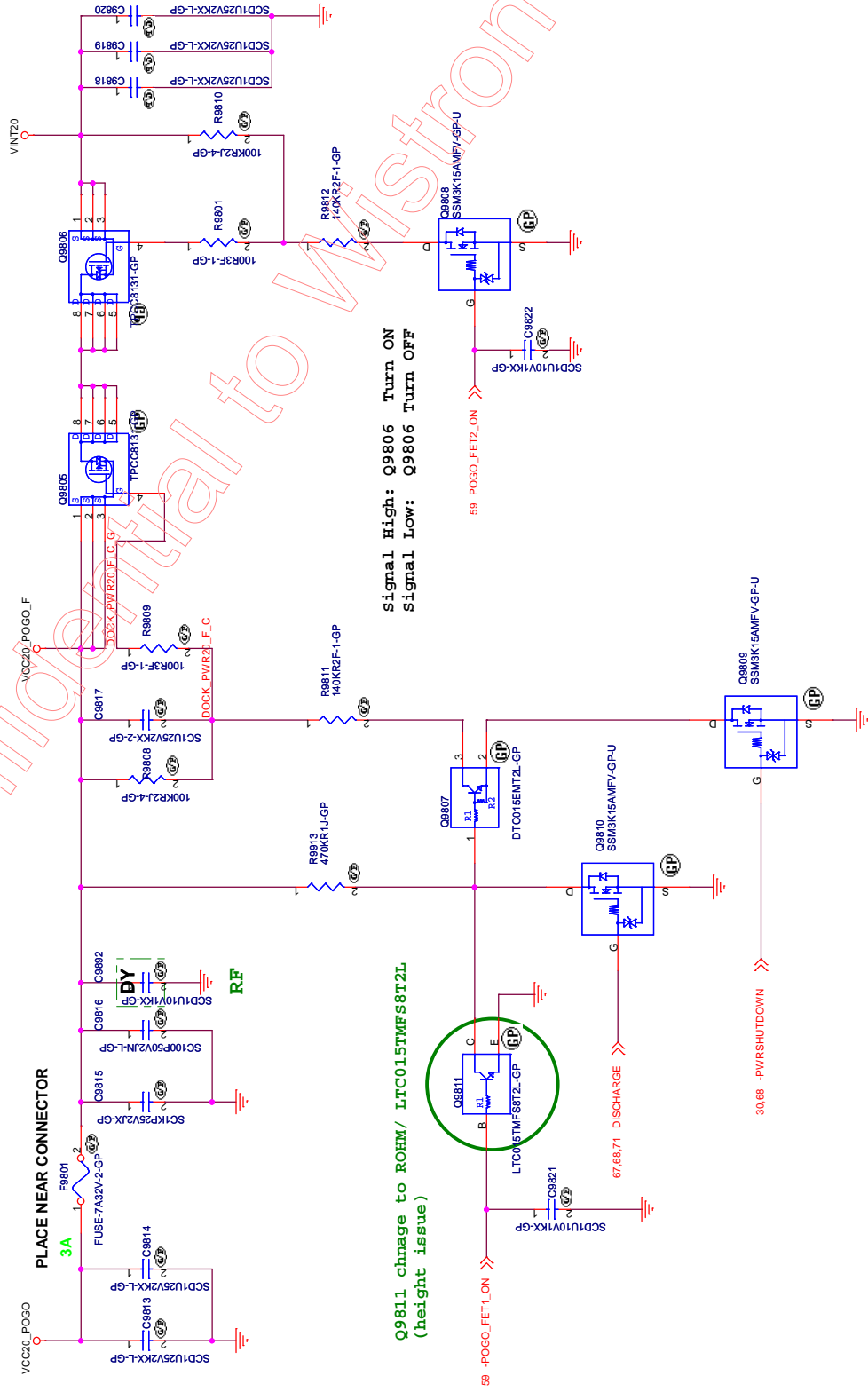
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Near to DCIN1



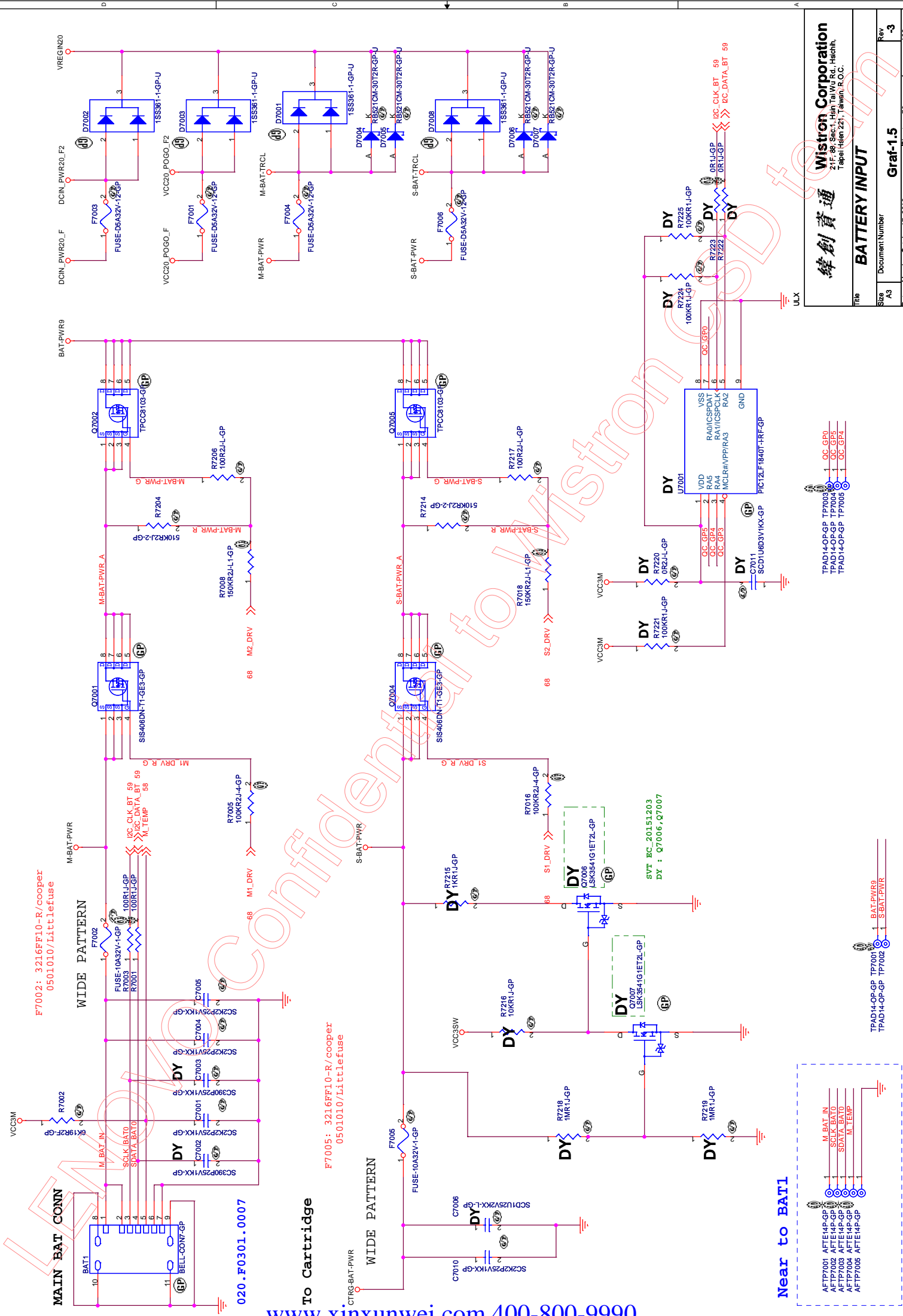
20.F2112.006

Total MLCC capacitance ad DCO connector is smaller then 1000pF to avoid LC resonance



Signal High: Q9806 Turn ON
Signal Low: Q9806 Turn OFF

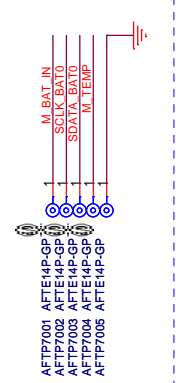
Q9811 change to ROHM/ LTC015TMF812L (height issue)



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BATTERY INPUT	
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Near to BAT1

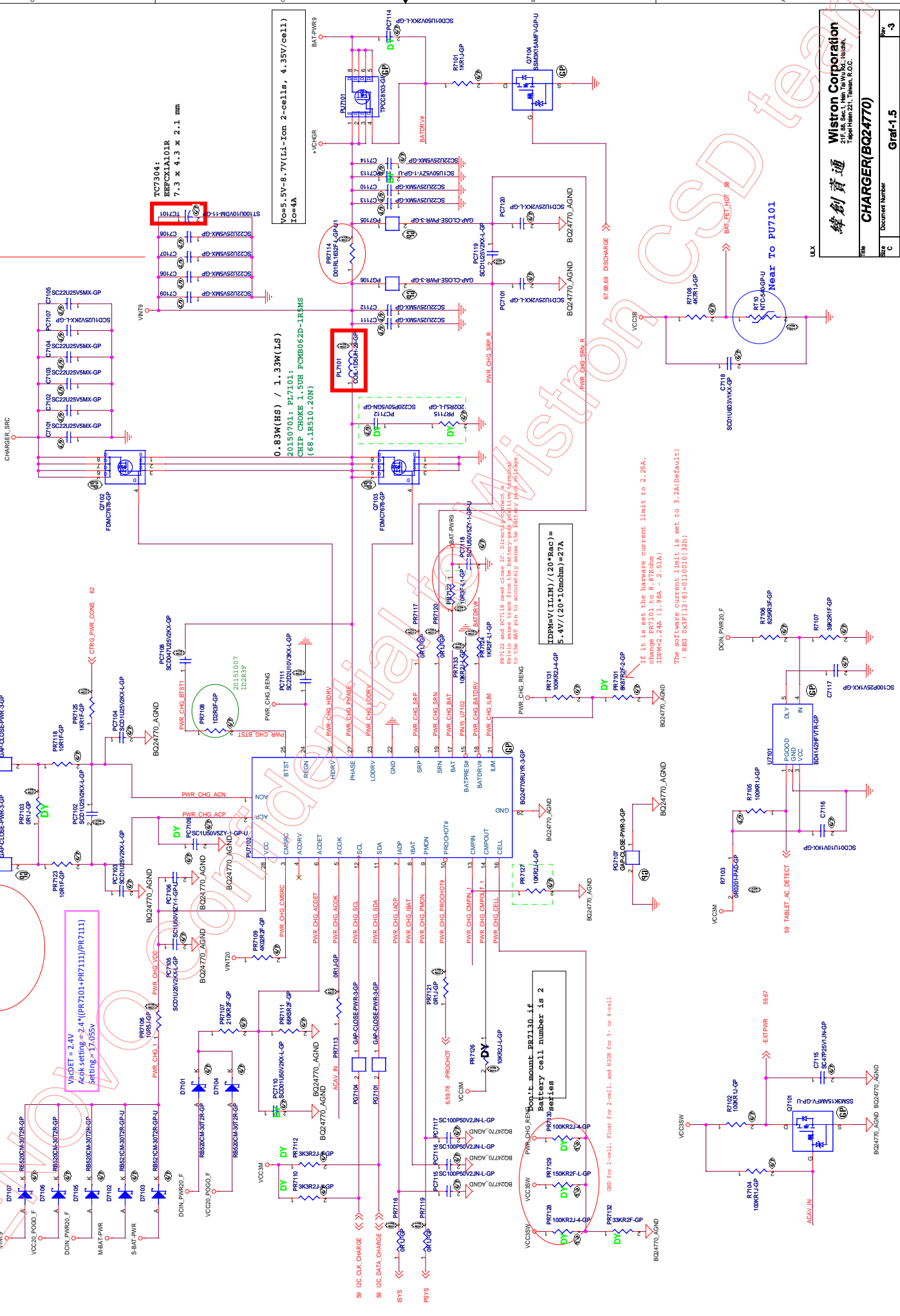


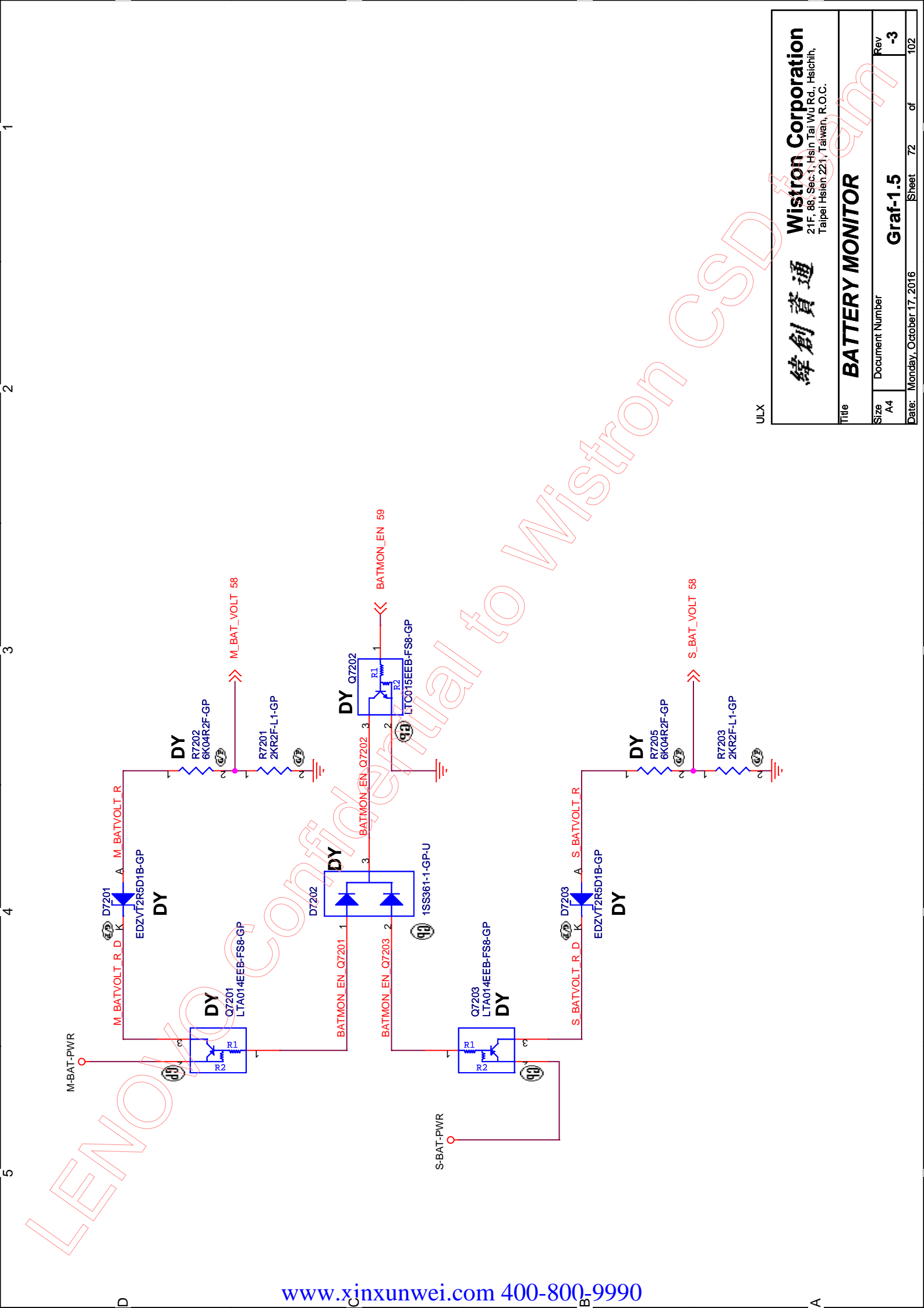
V_{REGN_REG} REGN Regulator Voltage V_{WCC} > 6.5V, V_{ACDET} > 0.6V

V_{IN} = 20V(2.25A) --- USB PD

Need confirm this two resistance ratio for charger setting

V_{ACDET} = 2.4V
Acik setting = 2.4 * ((PR7101 + PR7111) / PR7111)
Setting = 17.055V





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D

D

Power NexFET

Vin=5.5V-8.7V

Vin=5.5V-8.7V

DUAL-N Power-pak 3*3

D

D



Io=10A

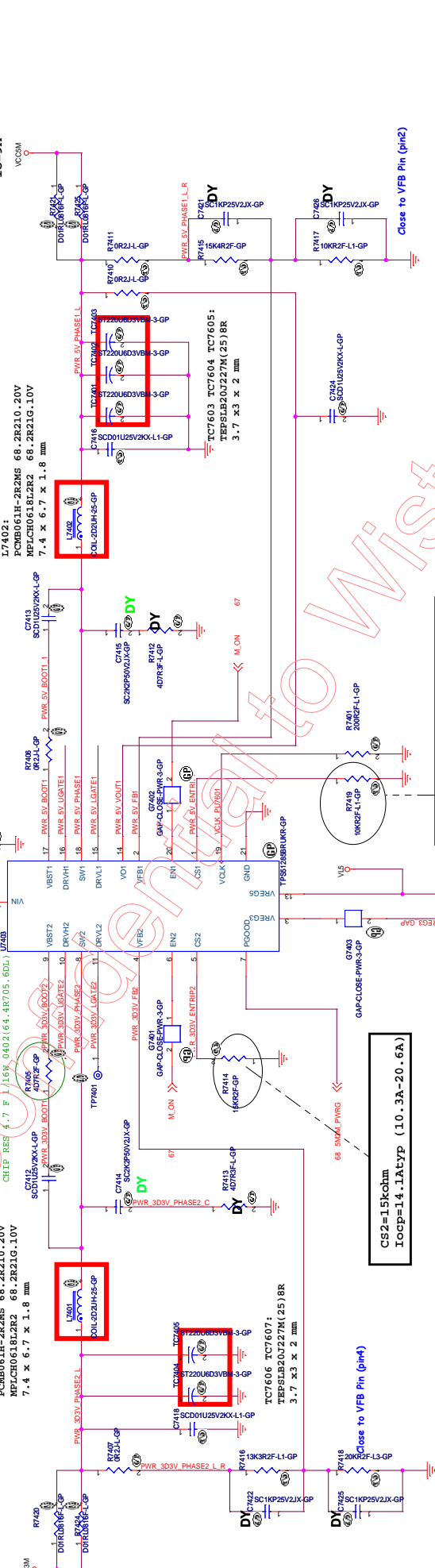
I_{max} = 10A

I_{tdc} = 5A

L7401:
PCMB061H-2R2M5 68.2R210.20V
MPLCH0618L2R2 68.2R21G.10V
7.4 x 6.7 x 1.8 mm

L7402:
PCMB061H-2R2M5 68.2R210.20V
MPLCH0618L2R2 68.2R21G.10V
7.4 x 6.7 x 1.8 mm

I_{max} = 9A
I_{tdc} = 5A
Io=9A



CS2=15kohm
Iocp=14.1A typ (10.3A-20.6A)

CS1=10kohm
Iocp=17.7A typ (15.5A-22.2A)

Close to VFB Pin (pin2)

Close to VFB Pin (pin4)

C

C

B

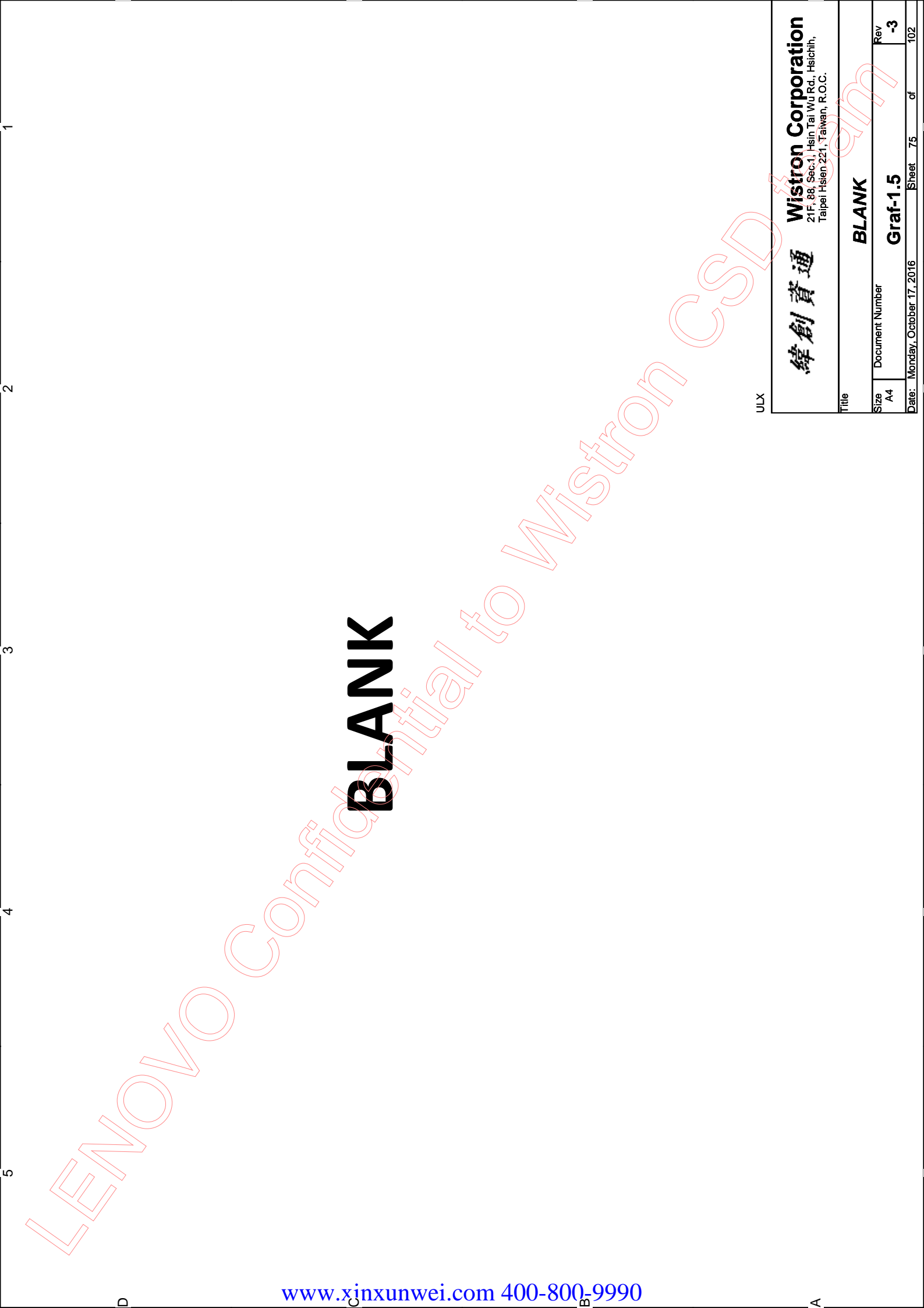
B

A

A

UT

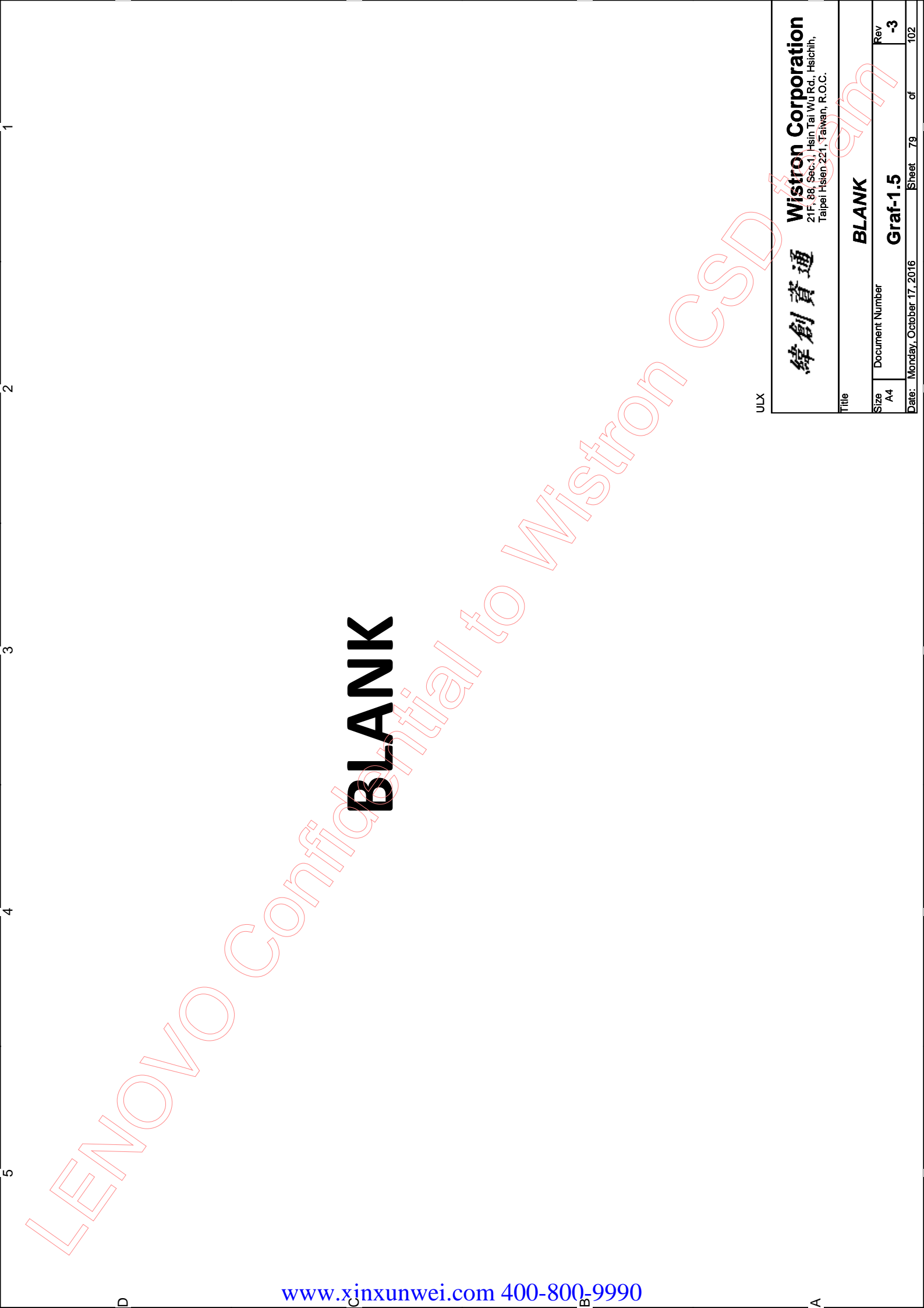
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VCC5M/VCC3M (TPS51285)		Document Number	
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Need confirm effective capacitance.

Note: R8007 should be 0ohm if remote sense is not used.

These sense lines should be routed as differential signals.

change to NB682GD-C669

TABLE : NB681 MODE M1 (0 to GND)

LP#	C1	C0	VOUT
0	X	X	0.000V
1	0	0	0.850V
1	0	1	0.875V
1	1	0	0.950V
1	1	1	0.975V

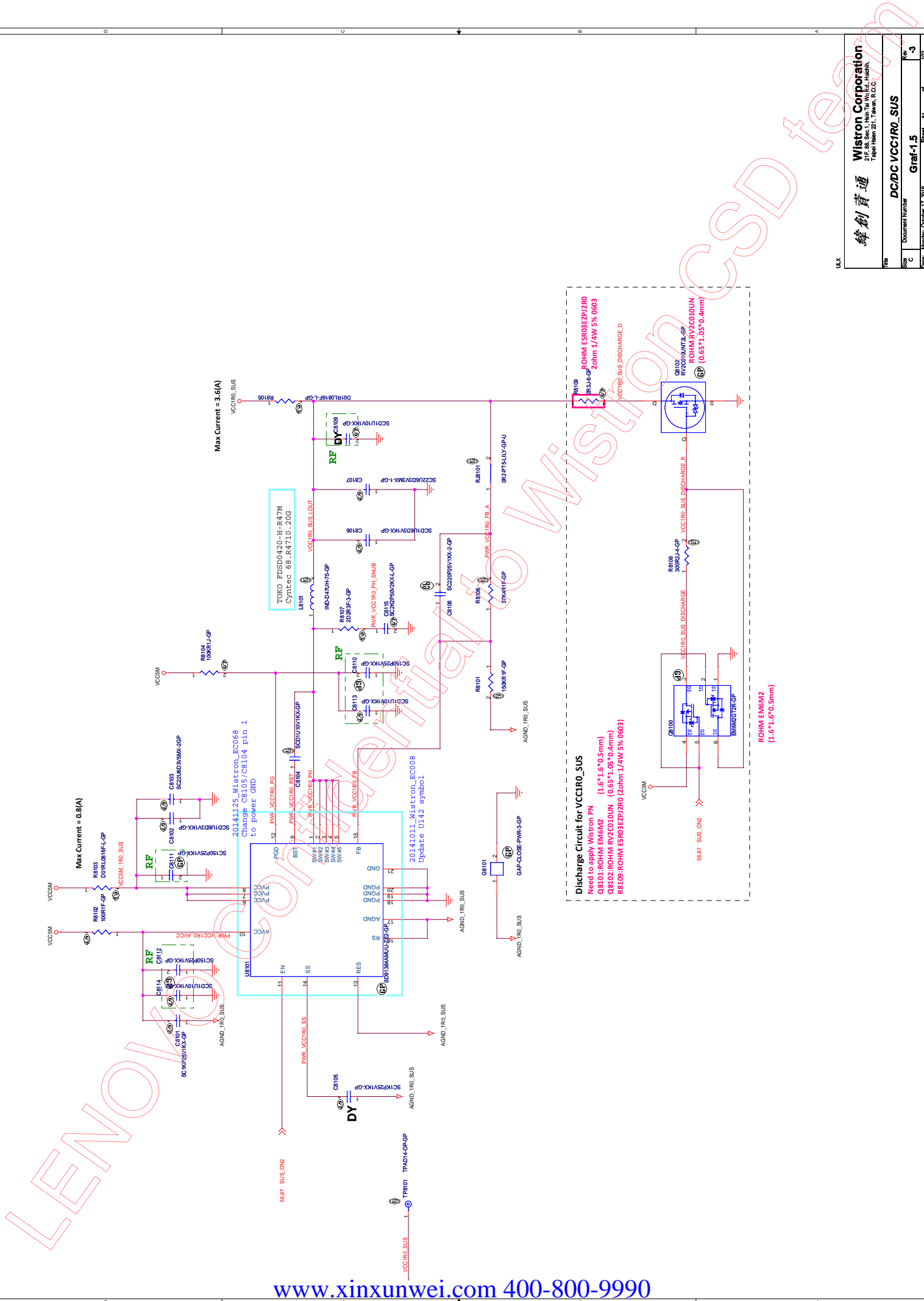
SLP_S0#

LOGIC

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Tapei (Hsin 22), Taiwan, R.O.C.

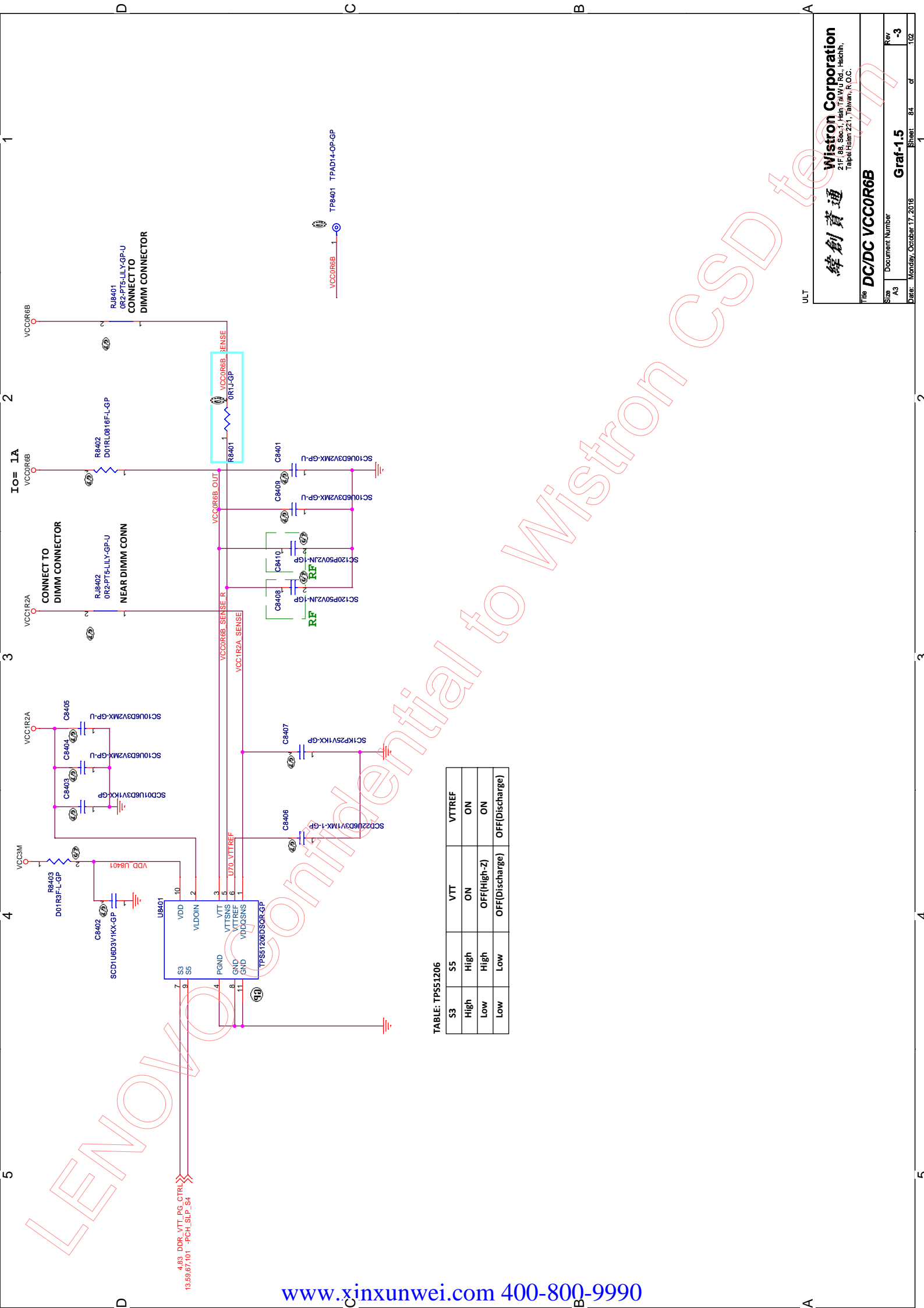
DC/DC VCCCPUIO(NB681)		
File	Document Number	Rev
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13.X

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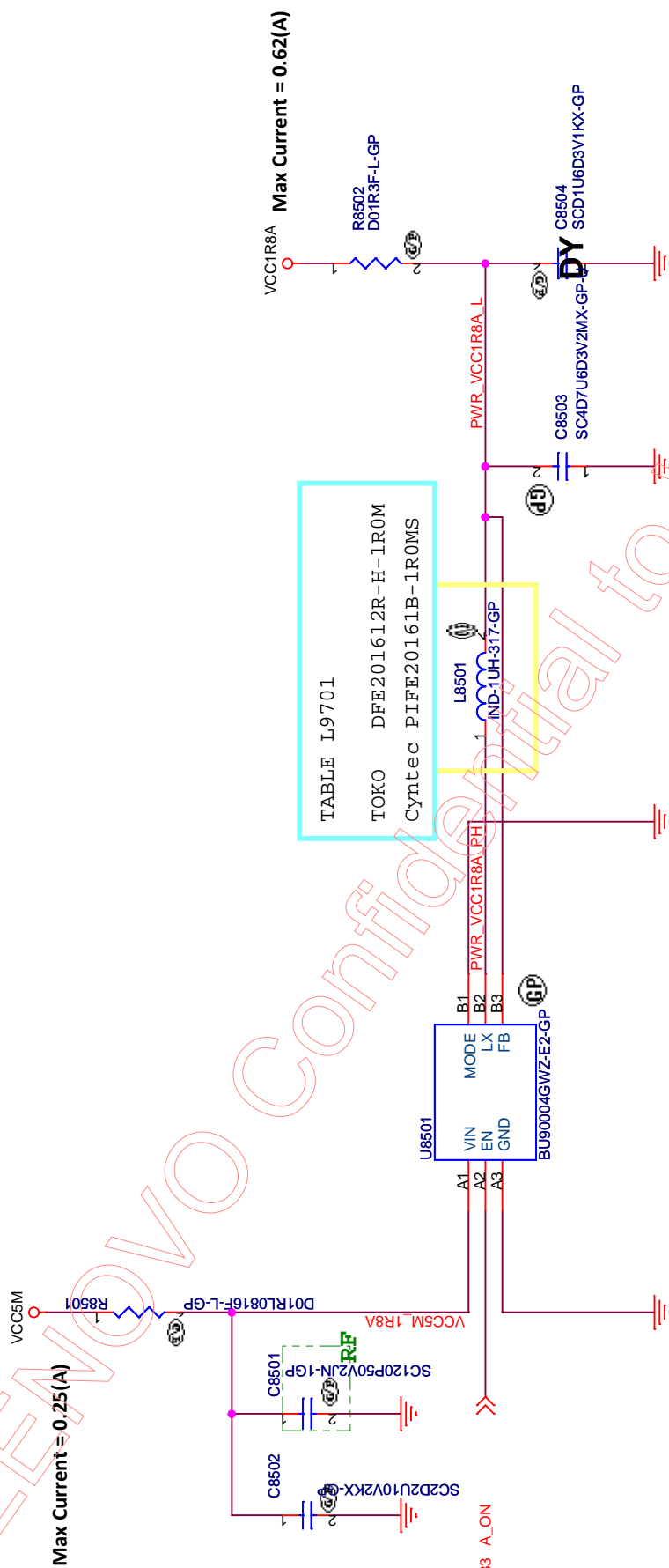
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3	DC/DC VCC1R0_SUS	3
C	Grat-1.5	
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DC/DC VCC0R6B			
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DC/DC VCC1R8A

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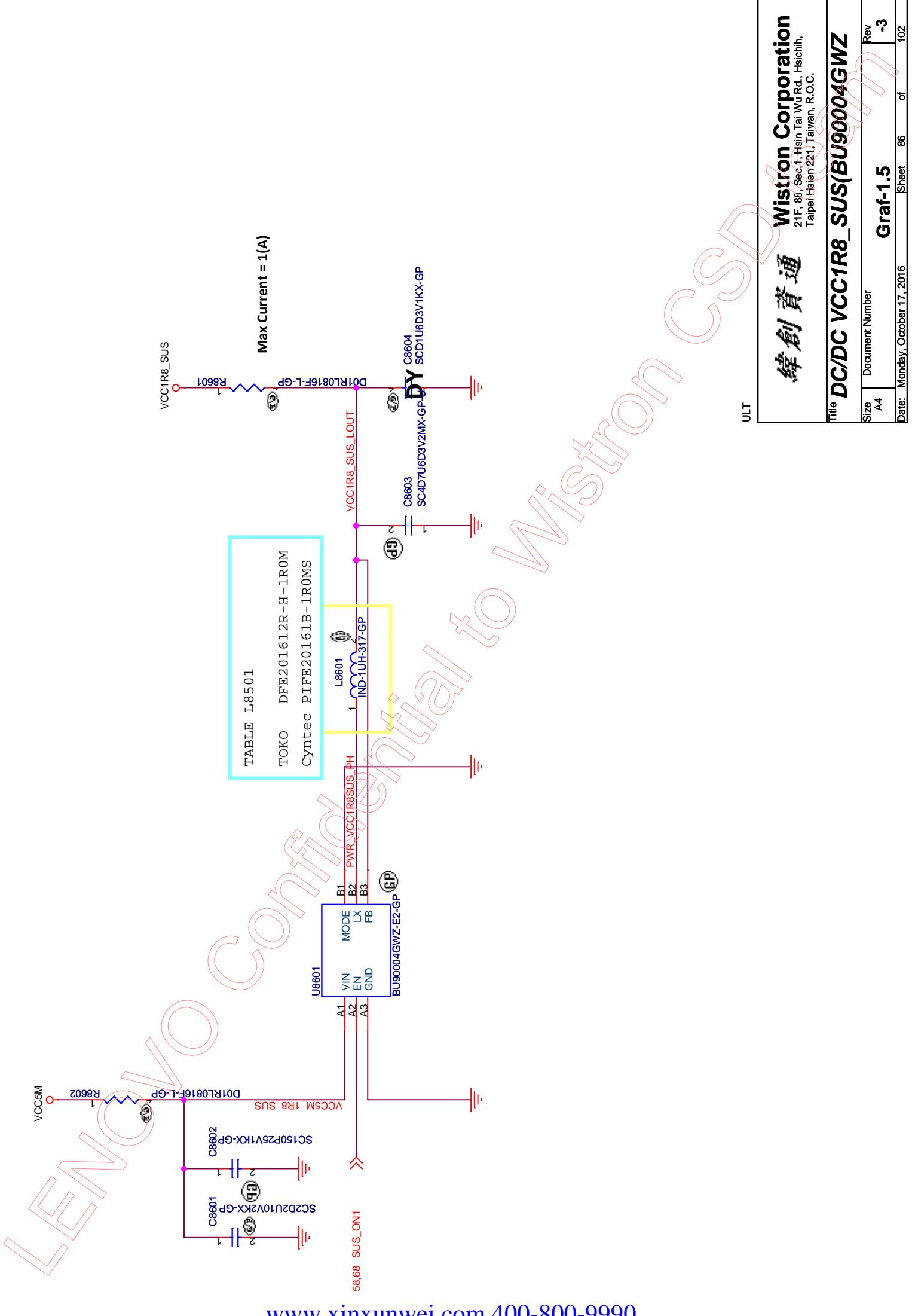
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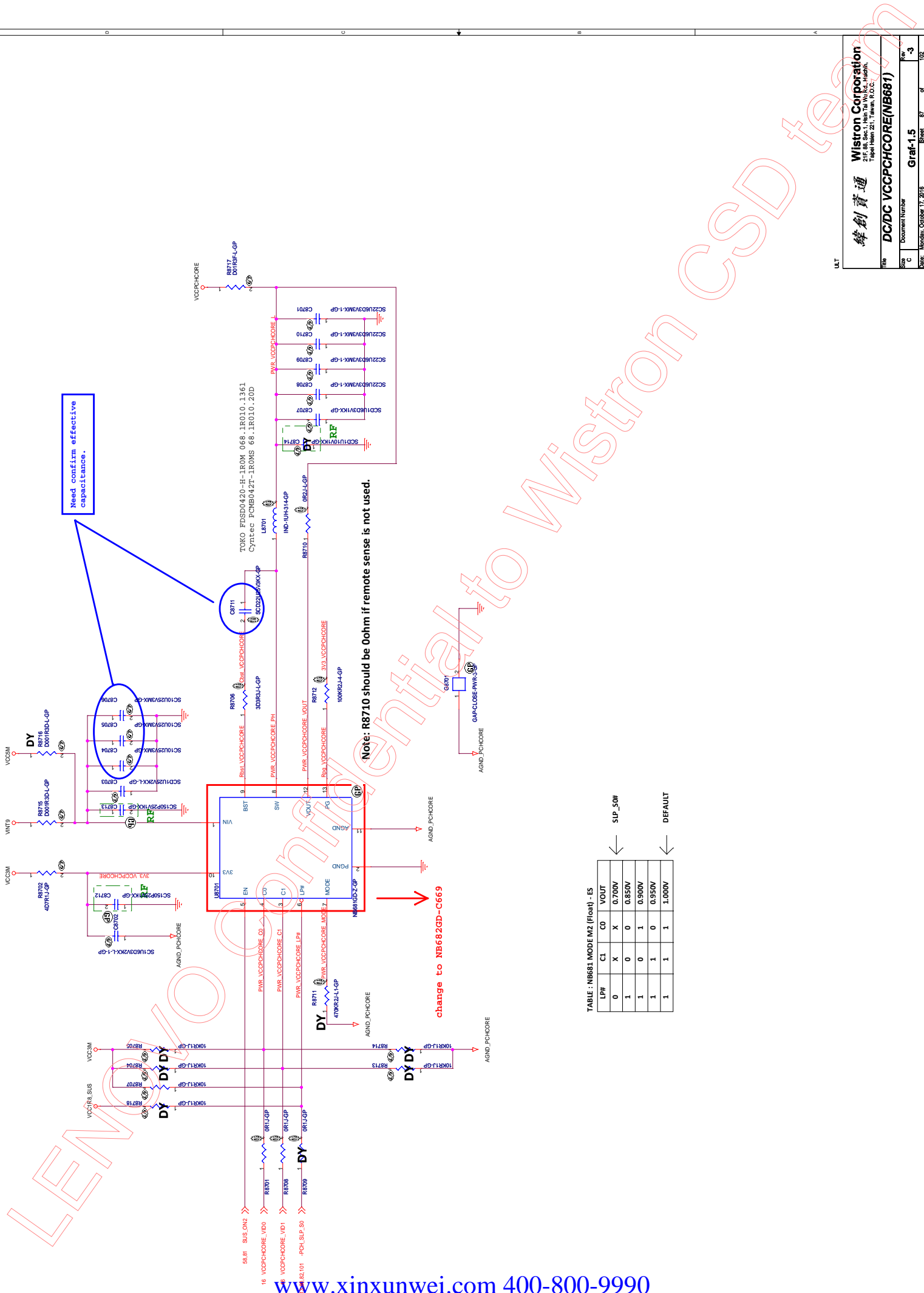
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DC/DC VCC1R8_SUS(BU90004GWZ)

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1.1

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DC/DC VCCPCHCORE(NB681)
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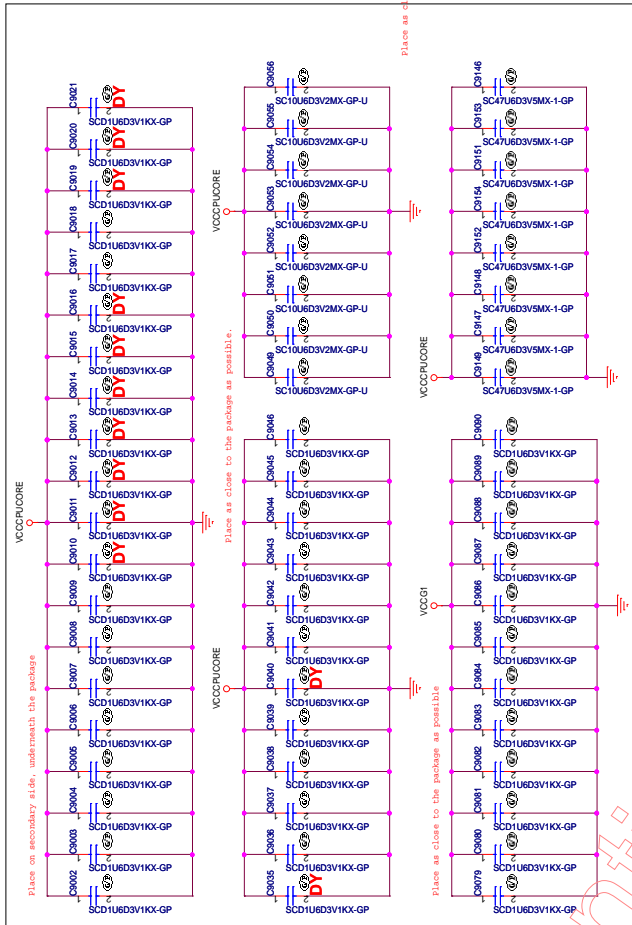
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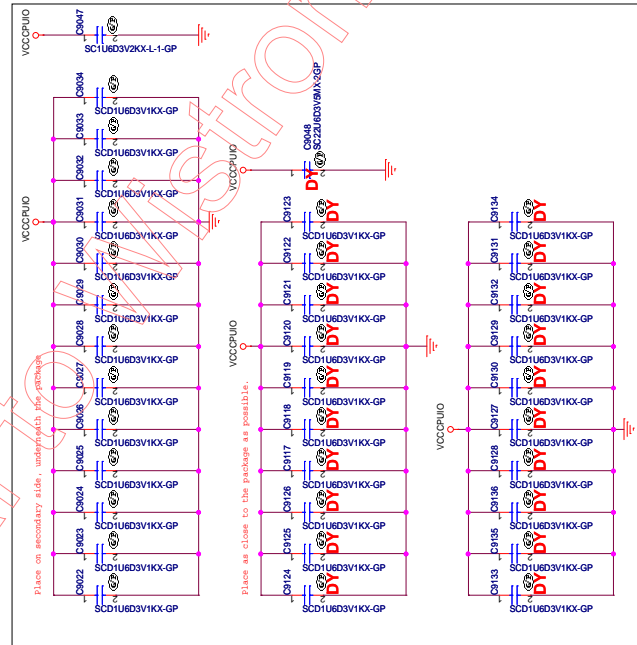
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Title			
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VCC_CORE

Package edge > 0402 caps > 0805 caps > Power source



Package edge > 0402 caps > 0805 caps > Power source



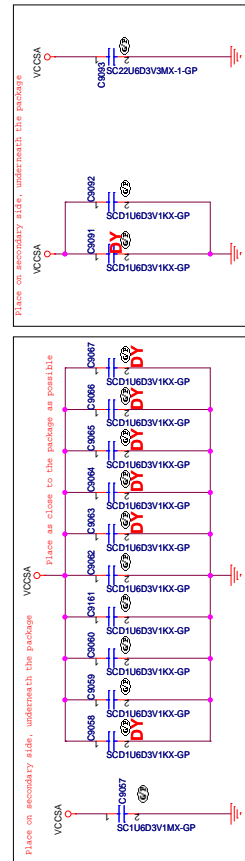
VCCGT

Package edge > 0402 caps > 0805 caps > Power source



VCCSA & VCCSA_DDR

Package edge > 0402 caps > 0805 caps > Power source



LT

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DC/DC Decoupling capacitor

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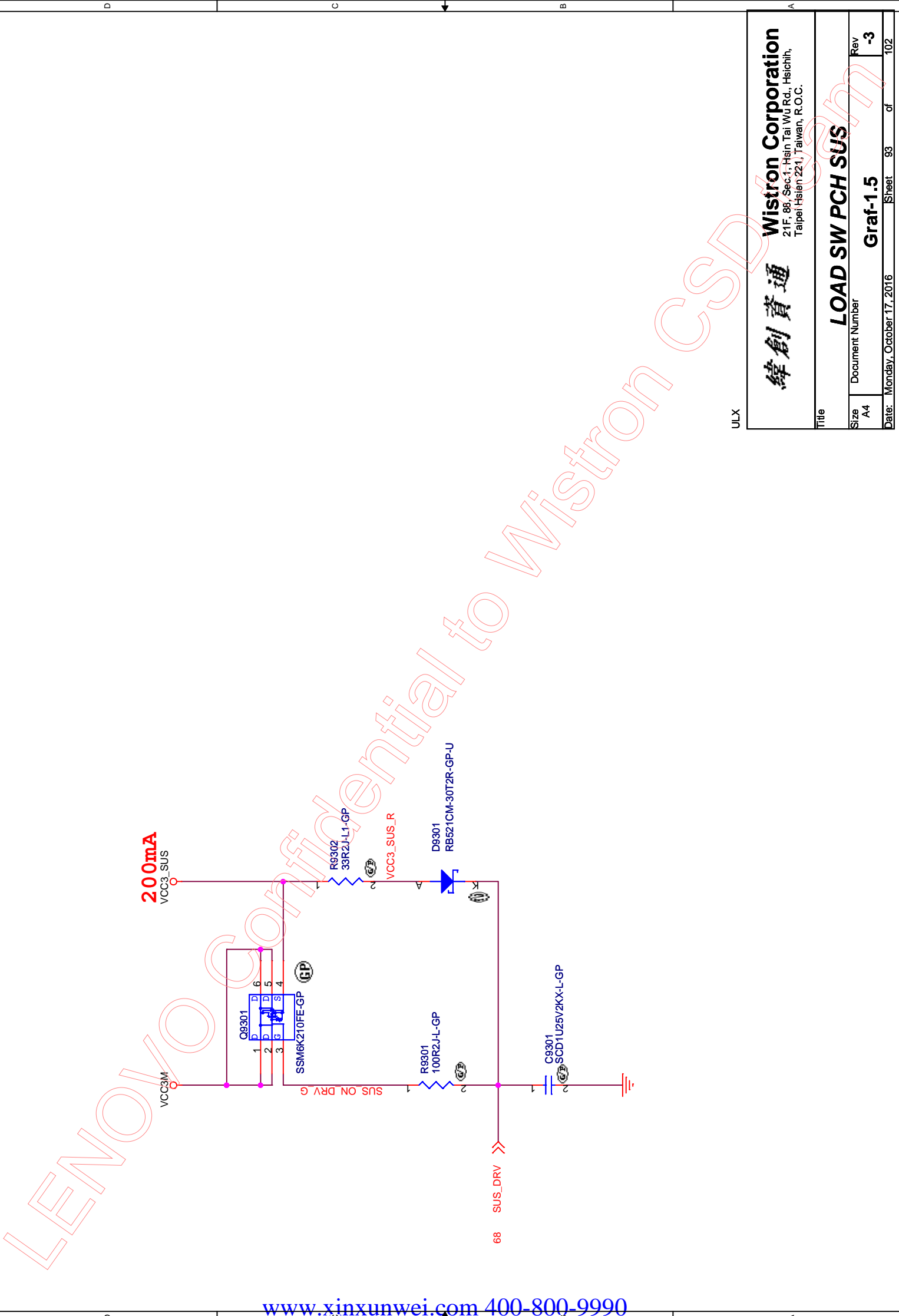
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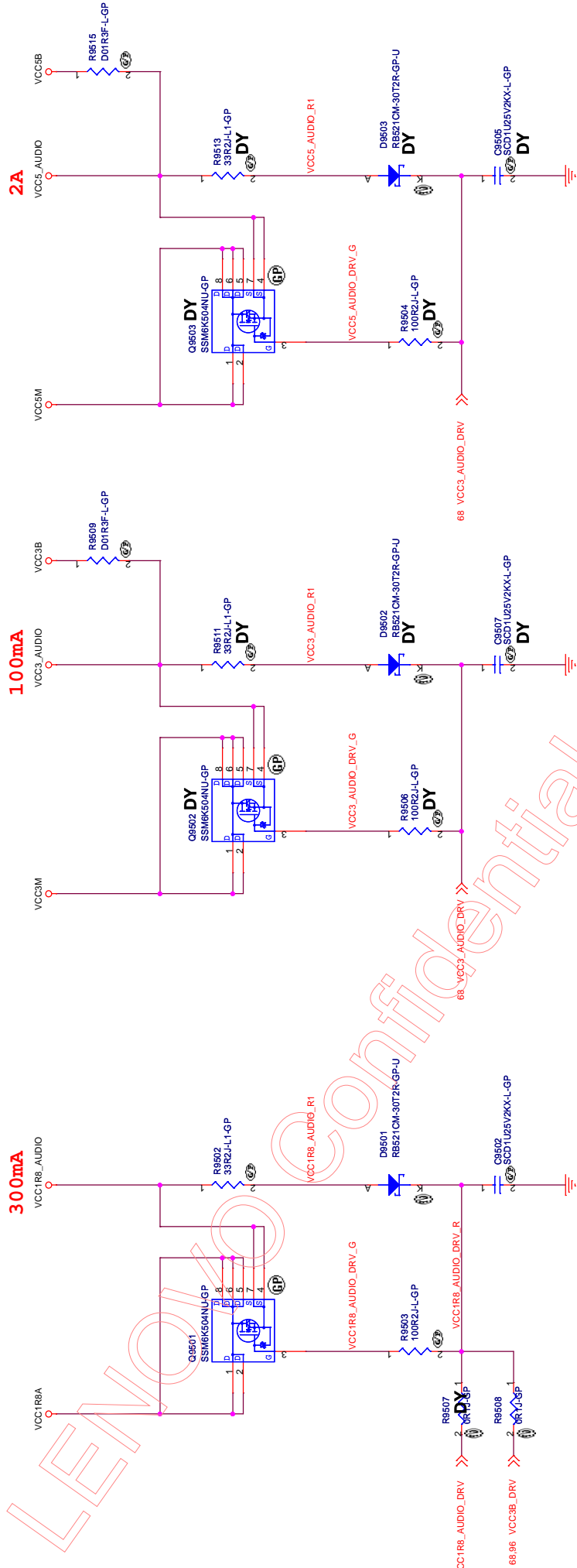
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LOAD SW PCH SUS

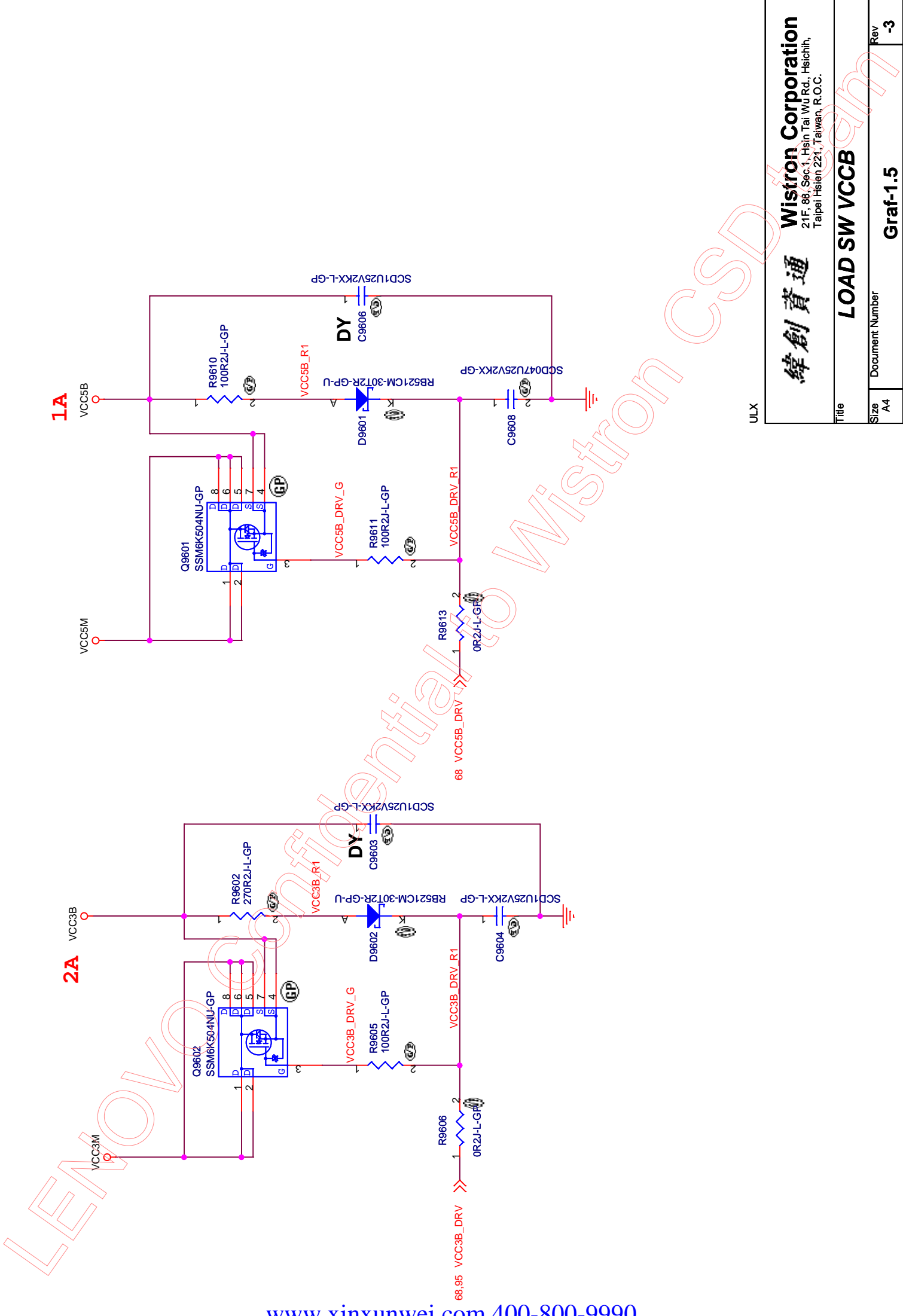
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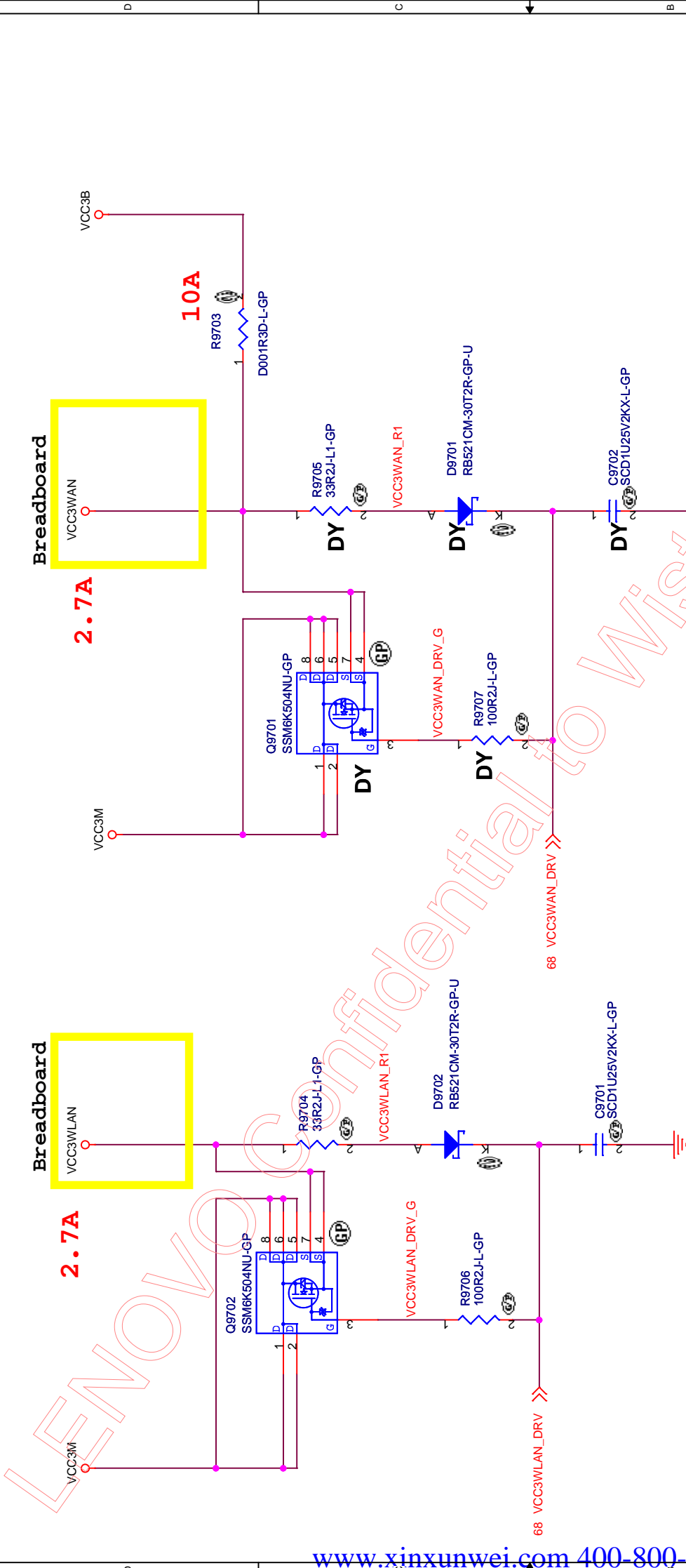


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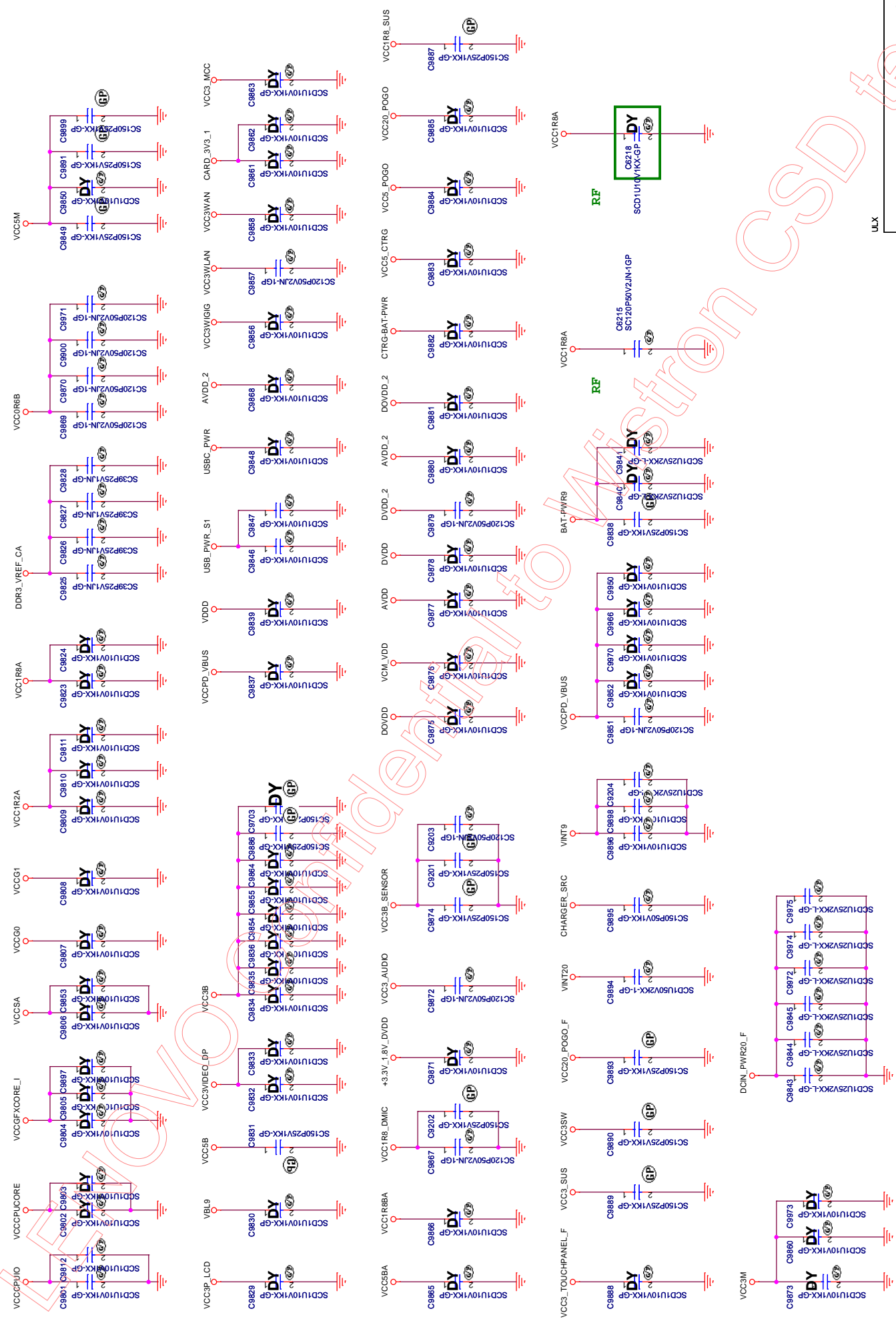
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Title			
LOAD SW VCCB			
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TABLE

AOAC	YES	NO
R9703	NO-ASM	ASM
Q9701	ASM	NO-ASM
R9705	ASM	NO-ASM
R9707	ASM	NO-ASM
C9702	ASM	NO-ASM
D9701	ASM	NO-ASM



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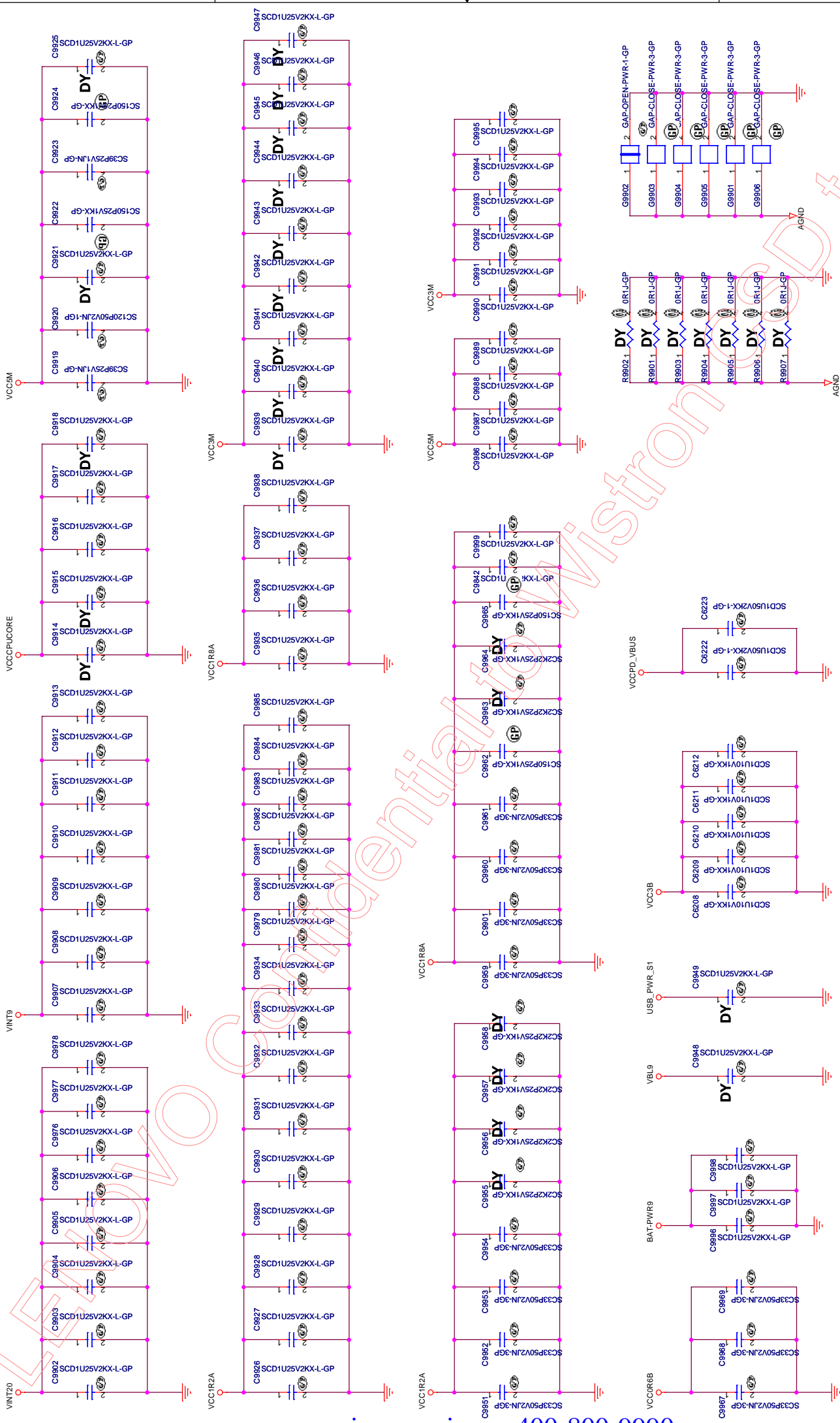
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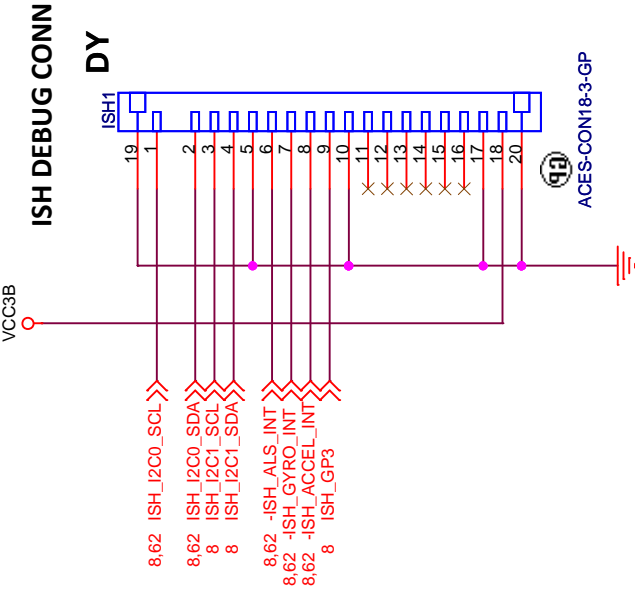
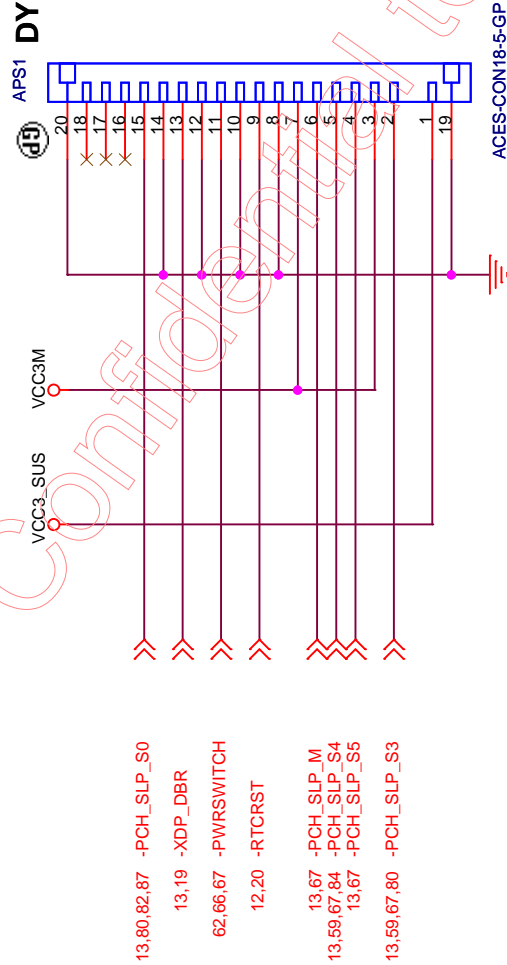
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APS/PETS Interface



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APS & ISH Connector

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Document Number

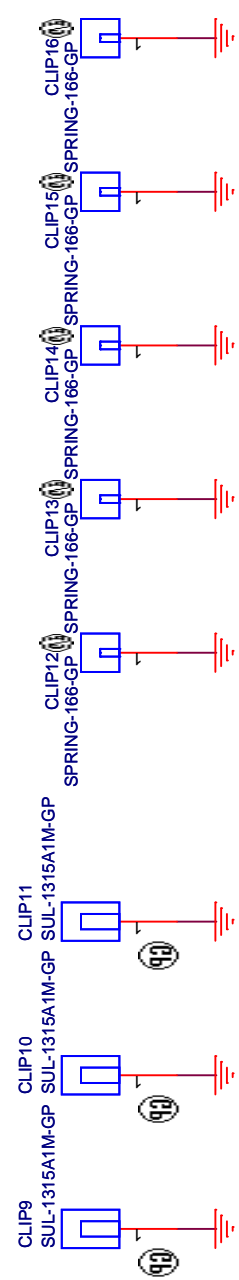
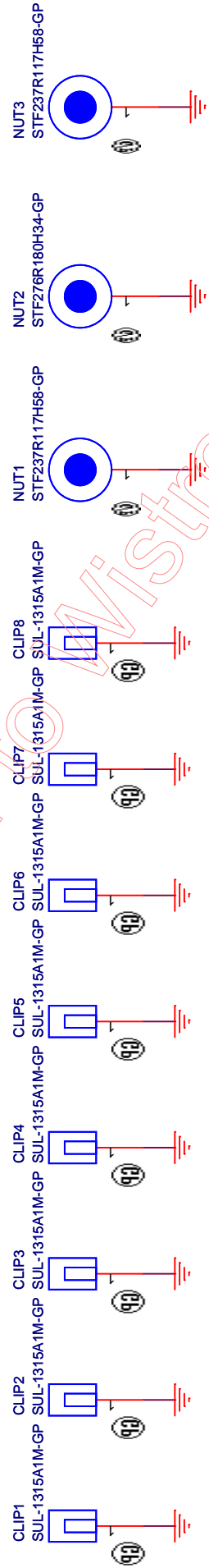
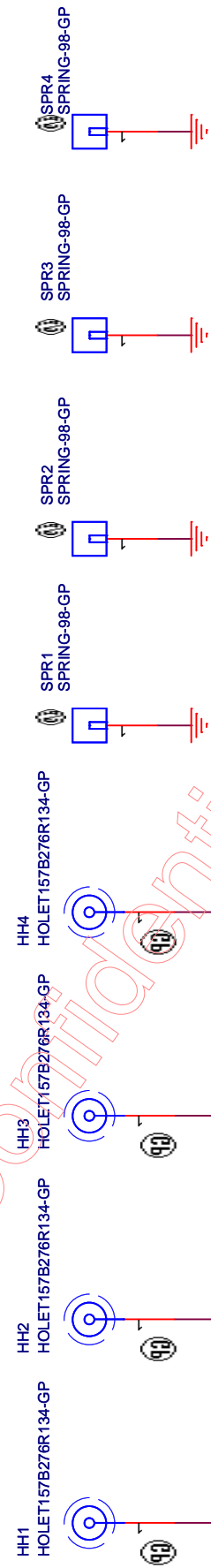
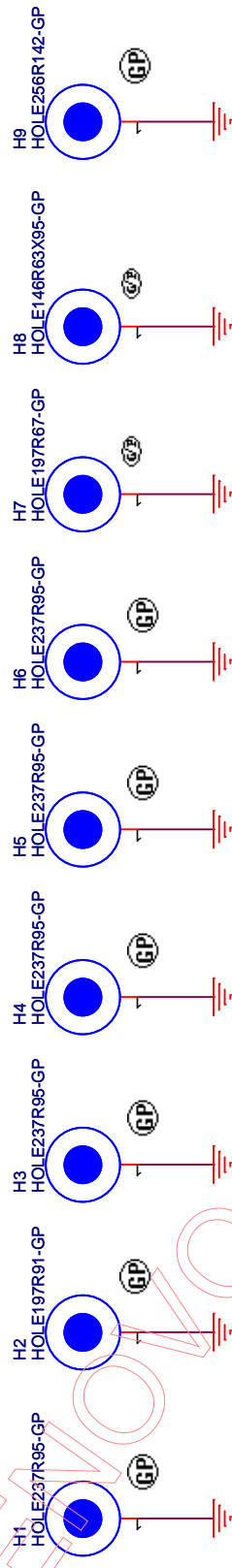
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SCREW HOLES	
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